



# MP2664

## 500mA, 5V USB, I<sup>2</sup>C-Controlled Battery Charger with Power Path Management for Single-Cell Li-Ion Battery in QFN Package

### DESCRIPTION

The MP2664 is a highly integrated, single-cell, Li-ion/Li-polymer battery charger with system power path management for space-limited, portable applications. The MP2664 uses input power from either an AC adapter or a USB port to supply the system load and charge the battery independently. The charger features constant current pre-charge, constant current fast-charge (CC) and constant voltage (CV) regulation, charge termination, and charge status.

The power path management function ensures continuous power to the system by automatically selecting the input, the battery, or both to power the system. This power stage features a low dropout regulator from the input to the system and a 100mΩ switch from the battery to the system. Power path management separates the charging current from the system load, which allows for proper charge termination and keeps the battery in full-charge mode.

The MP2664 provides system short-circuit protection (SCP) by limiting the current from the input to the system and the battery to the system. This feature is especially critical for preventing the Li-ion battery from being damaged by excessively high currents. An on-chip battery under-voltage lockout (UVLO) cuts off the path between the battery and the system if the battery voltage drops below the programmable battery UVLO threshold, which prevents the Li-ion battery from being over-discharged. An integrated I<sup>2</sup>C control interface allows the MP2664 to program the charging parameters, such as input current limit, input voltage regulation limit, charging current, battery regulation voltage, safety timer, and battery UVLO.

The MP2664 is available in a QFN-10 (2mmx2mm) package.

### FEATURES

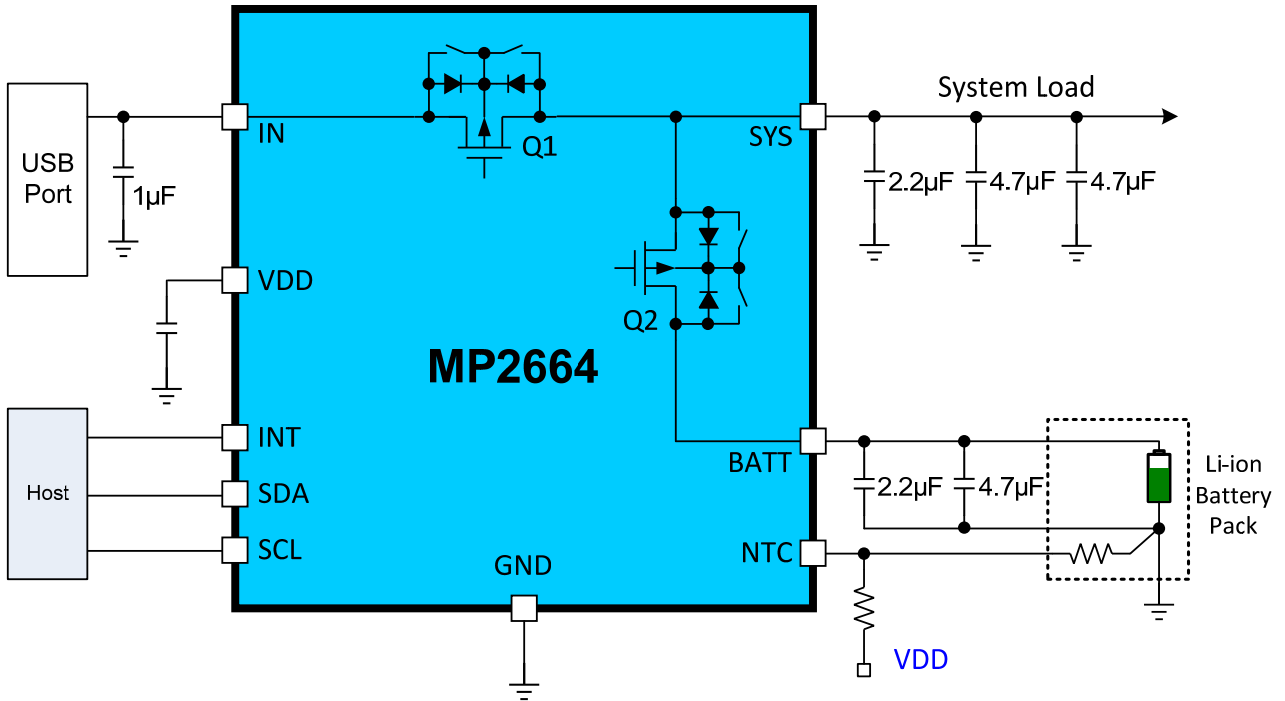
- Fully Autonomous Charger for Single-Cell Li-Ion/Li-Polymer Batteries
- Complete Power Path Management for Simultaneously Powering the System and Charging the Battery
- ±0.5% Charging Voltage Accuracy
- 13V Maximum Voltage for the Input Source
- I<sup>2</sup>C Interface for Setting Charging Parameters and Status Reporting
- Fully Integrated Power Switches and No External Blocking Diode Required
- Built-In Robust Charging Protection Including Battery Temperature Monitoring and Programmable Timer
- PCB Over-Temperature Protection (OTP)
- System Reset Function
- Built-In Battery Disconnection Function
- Thermal Limiting Regulation On-Chip
- Available in a QFN-10 (2mmx2mm) Package

### APPLICATIONS

- Wearable Devices
- Smart Handheld Devices
- Fitness Accessories
- Smart Watches

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TYPICAL APPLICATION



**ORDERING INFORMATION**

| Part Number*    | Package          | Top Marking |
|-----------------|------------------|-------------|
| MP2664GG-xxxx** | QFN-10 (2mmx2mm) | See Below   |
| EVKT-MP2664     | Evaluation Kit   | See Below   |

\* For Tape & Reel, add suffix -Z (e.g.: MP2664GG-xxxx-Z).

\*\*“xxxx” is the register setting option. The factory default is “0000.” This content can be viewed in the I<sup>2</sup>C register map. Please contact an MPS FAE to obtain an “xxxx” value.

**TOP MARKING**

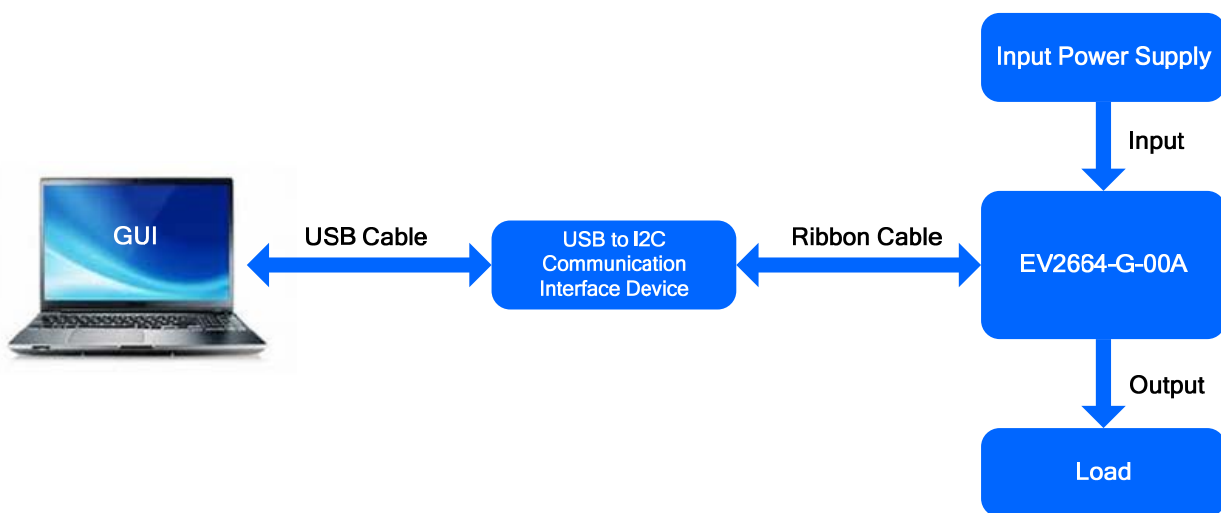
—  
**HVY**  
**LLL**

HV: Product code of MP2664GG  
 Y: Year code  
 LLL: Lot number

**EVALUATION KIT EVKT-MP2664**

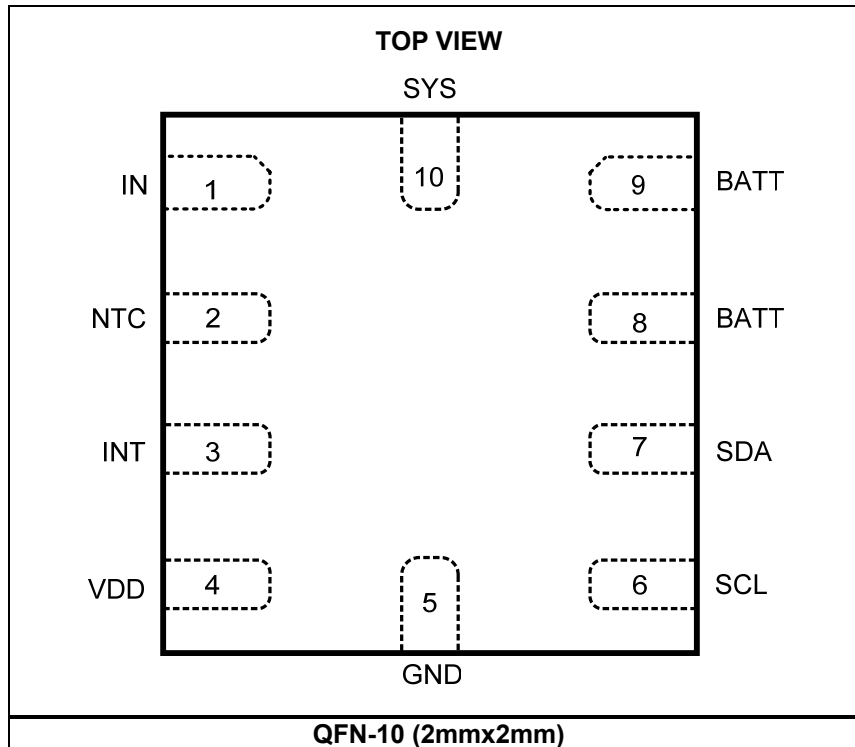
EVKT-MP2664 Kit contents: (Items below can be ordered separately)

| # | Part Number         | Item  | Quantity |
|---|---------------------|---|----------|
| 1 | EV2664-G-00A        | MP2664 evaluation board   | 1        |
| 2 | EVKT-USB2I2C-02-Bag | Includes one USB to I2C communication interface device, one USB cable, one ribbon cable | 1        |
| 3 | Online resources    | Includes: Datasheet, User guide, Product brief, and GUI                                 | 1        |



**EVKT-MP2664 Evaluation Kit Set-Up**

### PACKAGE REFERENCE



### PIN FUNCTIONS

| Package Pin # | Name | I/O   | Description  |
|---------------|------|-------|--|
| 1             | IN   | Power | <b>Input power.</b> Place a $\geq 1\mu\text{F}$ ceramic capacitor from IN to GND as close to the IC as possible.   |
| 2             | NTC  | I     | <b>Temperature sense input.</b> Connect a negative temperature coefficient thermistor to NTC. Program the hot and cold temperature window with a resistor divider from VDD to NTC to GND. The charge is suspended when NTC is out of range.  |
| 3             | INT  | O     | <b>Open-drain interrupt output.</b> INT can send the charging status and fault interruption to the host. INT is also used to disconnect the system from the battery. Pull INT from high to low for $>16\text{s}$ . The battery MOSFET is off and turns on automatically after $>4\text{s}$ regardless of the INT state. The external pull-up resistor at INT should <i>not</i> be smaller than $300\text{k}\Omega$ . |
| 4             | VDD  | I     | <b>Internal control power supply.</b> Connect a $0.1\mu\text{F}$ ceramic capacitor from VDD to GND. No external load is allowed.   |
| 5             | GND  | Power | <b>Ground.</b>   |
| 6             | SCL  | I/O   | <b>I<sup>2</sup>C interface clock.</b> Connect SCL to the logic rail through a $10\text{k}\Omega$ resistor.  |
| 7             | SDA  | I/O   | <b>I<sup>2</sup>C interface data.</b> Connect SDA to the logic rail through a $10\text{k}\Omega$ resistor.   |
| 8, 9          | BATT | Power | <b>Battery.</b> Place a ceramic capacitor from BATT to GND as close to the IC as possible.   |
| 10            | SYS  | Power | <b>System power supply.</b> Place a ceramic capacitor from SYS to GND as close to the IC as possible.  |

**ABSOLUTE MAXIMUM RATINGS** <sup>(1)</sup>

|  |                 |
|--|-----------------|
| V <sub>IN</sub> .....  | -0.3V to +13V   |
| All other pins to GND .....  | -0.3V to +6.0V  |
| Continuous power dissipation (T <sub>A</sub> = +25°C) <sup>(2)</sup> |                 |
| .....  | 1.25W           |
| Junction temperature .....   | 150°C           |
| Lead temperature (solder) .....                                      | 260°C           |
| Storage temperature .....  | -65°C to +150°C |

**Recommended Operating Conditions** <sup>(3)</sup>

|   |                         |
|---|-------------------------|
| Supply voltage (V <sub>IN</sub> ) .....         | 4.35V to 5.5V           |
|   | (USB input)             |
| I <sub>IN</sub> .....                           | Up to 455mA             |
| I <sub>SYS</sub> .....                          | Up to 3A <sup>(5)</sup> |
| I <sub>CHG</sub> .....                          | Up to 455mA             |
| V <sub>BATT</sub> .....                         | Up to 4.545V            |
| Operating junction temp. (T <sub>J</sub> )..... | -40°C to +125°C         |

|  |                       |                       |      |
|--|-----------------------|-----------------------|------|
| <b>Thermal Resistance</b> <sup>(4)</sup> | <b>θ<sub>JA</sub></b> | <b>θ<sub>JC</sub></b> |      |
| QFN-10 (2mmx2mm).....                    | 80                    | 16                    | °C/W |

**NOTES:**

- 1) Exceeding these ratings may damage the device.
- 2) The maximum allowable power dissipation is a function of the maximum junction temperature T<sub>J</sub> (MAX), the junction-to-ambient thermal resistance θ<sub>JA</sub>, and the ambient temperature T<sub>A</sub>. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P<sub>D</sub> (MAX) = (T<sub>J</sub> (MAX)-T<sub>A</sub>)/θ<sub>JA</sub>. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- 3) The device is not guaranteed to function outside of its operating conditions.
- 4) Measured on JESD51-7, 4-layer PCB.
- 5) Guaranteed by design

**ELECTRICAL CHARACTERISTICS**
**V<sub>IN</sub> = 5.0V, V<sub>BATT</sub> = 3.5V, T<sub>A</sub> = +25°C, unless otherwise noted.**

| Parameter   | Symbol                 | Condition  | Min  | Typ  | Max  | Units |
|---|------------------------|--|------|------|------|-------|
| <b>Input Source and Battery Protection</b>              |                        |  |      |      |      |       |
| Input operation voltage                                 | V <sub>IN</sub>        |  | 4.35 | 5    | 5.5  | V     |
| Battery input voltage <sup>(6)</sup>                    | V <sub>BATT</sub>      |  |      |      | 4.5  | V     |
| Input over-voltage protection trigger threshold         | V <sub>IN_OVP</sub>    | Input rising threshold   | 5.85 | 6    | 6.15 | V     |
| Input over-voltage protection recover threshold         |                        |  |      | 350  |      | mV    |
| Input under-voltage lockout threshold                   | V <sub>IN_UVLO</sub>   | Input rising threshold   | 3.8  | 3.9  | 4.0  | V     |
| Input under-voltage lockout threshold hysteresis        |                        |  |      | 170  |      | mV    |
| Input vs. battery voltage headroom threshold            | V <sub>HDRM</sub>      | Input rising vs. battery   | 100  | 130  | 160  | mV    |
| Input vs. battery voltage headroom threshold hysteresis |                        |  |      | 85   |      | mV    |
| Battery under-voltage lockout threshold                 | V <sub>BATT_UVLO</sub> | I <sup>2</sup> C programmable range  | 2.4  |      | 3.1  | V     |
|   |                        | Falling, programmable, Reg01 bit[2:0] = 100  | 2.6  | 2.8  | 3.0  | V     |
| Battery under-voltage threshold hysteresis              |                        |  |      | 210  |      | mV    |
| Battery over-voltage protection threshold               | V <sub>BATT_OVP</sub>  | Rising, higher than V <sub>BATT_REG</sub>  |      | 130  |      | mV    |
| Battery over-voltage protection hysteresis              |                        |  |      | 70   |      |       |
| <b>Power Path Management</b>                            |                        |  |      |      |      |       |
| System regulation voltage                               | V <sub>SYS_REG</sub>   | V <sub>IN</sub> = 5.5V, I <sub>SYS</sub> = 10mA, I <sub>CHG</sub> = 0A                       | 4.55 | 4.65 | 4.75 | V     |
| Input current limit                                     | I <sub>IN_LIM</sub>    | Reg00 bit[2:0] = 000 - 85mA  | 65   | 75   | 85   | mA    |
|   |                        | Reg00 bit[2:0] = 001 - 130mA   | 102  | 116  | 130  |       |
|   |                        | Reg00 bit[2:0] = 100 - 265mA   | 230  | 247  | 265  |       |
|   |                        | Reg00 bit[2:0] = 111 - 455mA   | 400  | 428  | 455  |       |
| Input minimum voltage regulation                        | V <sub>IN_MIN</sub>    | I <sup>2</sup> C programmable range  | 3.88 |      | 5.08 | V     |
|   |                        | I <sup>2</sup> C setting V <sub>IN_MIN</sub> = 4.20V   | 4.10 | 4.20 | 4.30 |       |
| IN to SYS switch on resistance                          | R <sub>ON_Q1</sub>     | V <sub>IN</sub> = 5V, I <sub>SYS</sub> = 100mA   |      | 300  | 400  | mΩ    |
| Input quiescent current                                 | I <sub>IN_Q</sub>      | V <sub>IN</sub> = 5.5V, CE = L, charge enabled, I <sub>CHG</sub> = 0A, I <sub>SYS</sub> = 0A |      | 630  |      | μA    |
|   |                        | V <sub>IN</sub> = 5.5V, CE = H, charge disabled  |      | 500  |      |       |

**ELECTRICAL CHARACTERISTICS (continued)**
**V<sub>IN</sub> = 5.0V, V<sub>BATT</sub> = 3.5V, T<sub>A</sub> = +25°C, unless otherwise noted.**

| Parameter                                       | Symbol                | Condition   | Min   | Typ  | Max                 | Units |
|---|-----------------------|---|-------|------|---------------------|-------|
| Battery quiescent current                       | I <sub>BATT_Q</sub>   | V <sub>IN</sub> = 5V, CE = L, I <sub>SYS</sub> = 0A, V <sub>BATT</sub> = 4.3V   |       | 32   |                     | μA    |
|   |                       | V <sub>IN</sub> = 0V, CE = H, I <sub>SYS</sub> = 0A, V <sub>BATT</sub> = 4.35V, disable PCB OTP function, do not include the current from external NTC resistor |       | 11   | 13                  |       |
|   |                       | V <sub>IN</sub> = 0V, CE = H, I <sub>SYS</sub> = 0A, V <sub>BATT</sub> = 4.35V, enable PCB OTP function, do not include the current from external NTC resistor  |       | 20   | 24                  |       |
|   |                       | V <sub>BATT</sub> = 4.5V, V <sub>IN</sub> = V <sub>SYS</sub> = GND, FET_DIS = 1, shipping mode  |       | 4    | 5.5                 |       |
| Battery MOSFET on resistance                    | R <sub>ON_Q2</sub>    | V <sub>IN</sub> < 2V, V <sub>BATT</sub> = 3.5V, I <sub>SYS</sub> = 100mA  |       | 100  | 150                 | mΩ    |
| Battery current regulation in discharge mode    | I <sub>DSCHG</sub>    | I <sup>2</sup> C programmable range   | 400   |      | 3200 <sup>(6)</sup> | mA    |
| Battery MOSFET switch leakage                   |                       | V <sub>BATT</sub> = 4.5V, V <sub>IN</sub> = V <sub>SYS</sub> = GND, disconnect mode   |       |      | 1                   | μA    |
| SYS reverse to BATT switch leakage              |                       | V <sub>SYS</sub> = 6V, V <sub>IN</sub> = 4.5V, V <sub>BATT</sub> = GND, CE = H  |       |      | 1                   | μA    |
| Battery MOSFET disconnect by INT <sup>(6)</sup> | t <sub>INT</sub>      | INT pull-low lasting time to turn off the battery MOSFET  |       | 16   |                     | s     |
|   |                       | Battery FET off lasting time before turn-on   |       | 4    |                     |       |
| <b>Battery Charger</b>                          |                       |   |       |      |                     |       |
| Battery charge voltage regulation               | V <sub>BATT_REG</sub> | I <sup>2</sup> C programmable range   | 3.600 |      | 4.545               | V     |
|   |                       | Reg04 bit[7:2] = 101000   | 4.179 | 4.20 | 4.221               |       |
|   |                       | Reg04 bit[7:2] = 110010   | 4.328 | 4.35 | 4.372               |       |
| Fast charge current                             | I <sub>CC</sub>       | V <sub>IN</sub> = 5V, V <sub>BATT</sub> = 3.8V, I <sup>2</sup> C programmable range   | 8     |      | 535 <sup>(6)</sup>  | mA    |
|   |                       | V <sub>IN</sub> = 5V, V <sub>BATT</sub> = 3.8V, I <sub>CC_SETTING</sub> = 93mA  | 88    | 93   | 98                  |       |
|   |                       | V <sub>IN</sub> = 5V, V <sub>BATT</sub> = 3.8V, I <sub>CC_SETTING</sub> = 246mA   | 232   | 248  | 263                 |       |
|   |                       | V <sub>IN</sub> = 5V, V <sub>BATT</sub> = 3.8V, I <sub>CC_SETTING</sub> = 399mA   | 376   | 401  | 440                 |       |
| Junction temperature regulation <sup>(6)</sup>  | T <sub>J_REG</sub>    | Reg06 bit[1:0] = 11 - 120°C   |       | 120  |                     | °C    |

**ELECTRICAL CHARACTERISTICS (continued)**
**V<sub>IN</sub> = 5.0V, V<sub>BATT</sub>=3.5V, T<sub>A</sub> = +25°C, unless otherwise noted.**

| Parameter  | Symbol                | Condition  | Min  | Typ  | Max | Units |
|--|-----------------------|--|------|------|-----|-------|
| Pre-charge current                               | I <sub>PRE</sub>      | I <sup>2</sup> C programmable range                                      | 6    |      | 27  | mA    |
|  |                       | I <sub>PRE_SETTING</sub> = 6mA, Reg03 bit[1:0] = 00                      | 2.5  | 4.7  |     |       |
|  |                       | I <sub>PRE_SETTING</sub> = 20mA, Reg03 bit[1:0] = 10                     | 14   | 18   | 22  |       |
| Charge termination current threshold             | I <sub>TERM</sub>     | I <sub>CC_SETTING</sub> ≤ 263mA, (Reg02 bit[4] = 0), Reg03 bit[1:0] = 00 | 5    | 7    | 9   | mA    |
|  |                       | I <sub>CC_SETTING</sub> ≤ 263mA, (Reg02 bit[4] = 0), Reg03 bit[1:0] = 01 | 10   | 13.5 | 17  |       |
|  |                       | I <sub>CC_SETTING</sub> ≤ 263mA, (Reg02 bit[4] = 0), Reg03 bit[1:0] = 10 | 16   | 20   | 24  |       |
|  |                       | I <sub>CC_SETTING</sub> ≤ 263mA, (Reg02 bit[4] = 0), Reg03 bit[1:0] = 11 | 22   | 27   | 32  |       |
|  |                       | I <sub>CC_SETTING</sub> ≤ 280mA, (Reg02 bit[4] = 1), Reg03 bit[1:0] = 00 | 10   | 13.5 | 17  |       |
|  |                       | I <sub>CC_SETTING</sub> ≤ 280mA, (Reg02 bit[4] = 1), Reg03 bit[1:0] = 01 | 22   | 27   | 32  |       |
|  |                       | I <sub>CC_SETTING</sub> ≤ 280mA, (Reg02 bit[4] = 1), Reg03 bit[1:0] = 10 | 34   | 42   | 49  |       |
|  |                       | I <sub>CC_SETTING</sub> ≤ 280mA, (Reg02 bit[4] = 1), Reg03 bit[1:0] = 11 | 46   | 55   | 64  |       |
| Charge termination current threshold hysteresis  | I <sub>TERM_HYS</sub> | I <sub>CC_SETTING</sub> ≤ 263mA, (Reg02 bit[4] = 0), Reg03 bit[1:0] = 10 | 7.5  | 11   | 15  | mA    |
|  |                       | I <sub>CC_SETTING</sub> ≤ 280mA, (Reg02 bit[4] = 0), Reg03 bit[1:0] = 10 | 19   | 25   | 31  |       |
| Pre-charge to fast charge threshold              | V <sub>BATT_PRE</sub> | V <sub>BATT</sub> rising, set V <sub>BATT_PRE</sub> = 3.0V               | 2.8  | 3.0  | 3.1 | V     |
| Pre-charge to fast charge threshold hysteresis   |                       |  |      | 90   |     | mV    |
| Auto-recharge battery voltage threshold          | V <sub>RECH</sub>     | Reg04 bit[0] = 0   | 120  | 160  | 200 | mV    |
|  |                       | Reg04 bit[0] = 1   | 260  | 300  | 365 |       |
| <b>Thermal Protection</b>                        |                       |  |      |      |     |       |
| Thermal shutdown threshold <sup>(6)</sup>        | T <sub>J_SHDN</sub>   | Rising   |      | 150  |     | °C    |
| Thermal shutdown hysteresis <sup>(6)</sup>       |                       |  |      | 20   |     | °C    |
| NTC output current                               | I <sub>NTC</sub>      | CE = L, NTC = 3V   | -100 | 0    | 100 | nA    |
| NTC cold temperature rising threshold            | V <sub>COLD</sub>     | As a percentage of V <sub>DD</sub>                                       | 63   | 65   | 67  | %     |
| NTC cold temperature rising threshold hysteresis |                       |  |      | 30   |     | mV    |



**ELECTRICAL CHARACTERISTICS (continued)**
**V<sub>IN</sub> = 5V, T<sub>A</sub> = 25°C, unless otherwise noted.**

| Parameter  | Symbol               | Condition                                | Min | Typ | Max | Units |
|--|----------------------|--|-----|-----|-----|-------|
| NTC hot temperature falling threshold                        | V <sub>HOT</sub>     | As a percentage of V <sub>DD</sub>       | 31  | 33  | 35  | %     |
| NTC hot temperature falling threshold hysteresis             |                      |  |     | 70  |     | mV    |
| NTC hot temperature falling threshold for PCB OTP            | V <sub>HOT_PCB</sub> | As a percentage of V <sub>DD</sub>       | 30  | 32  | 34  | %     |
| NTC hot temperature falling threshold hysteresis for PCB OTP |                      |  |     | 85  |     | mV    |
| <b>Logic I/O Pin Characteristics</b> <sup>(6)</sup>          |                      |  |     |     |     |       |
| Low logic voltage threshold                                  | V <sub>L</sub>       |  |     |     | 0.4 | V     |
| High logic voltage threshold                                 | V <sub>H</sub>       |  | 1.3 |     |     | V     |
| <b>I<sup>2</sup>C Interface (SDA, SCL)</b> <sup>(6)</sup>    |                      |  |     |     |     |       |
| Input high voltage level                                     | V <sub>IH</sub>      | V <sub>PULL_UP</sub> = 1.8V, SDA and SCL | 1.3 |     |     | V     |
| Input low voltage level                                      | V <sub>IL</sub>      | V <sub>PULL_UP</sub> = 1.8V, SDA and SCL |     |     | 0.4 | V     |
| Output low voltage level                                     | V <sub>OL</sub>      | I <sub>SINK</sub> = 5mA                  |     |     | 0.4 | V     |
| I <sup>2</sup> C clock frequency                             | F <sub>SCL</sub>     |  |     |     | 400 | kHz   |
| <b>Clock Frequency and Watchdog Timer</b>                    |                      |  |     |     |     |       |
| Clock frequency  | F <sub>CLK</sub>     |  |     | 32  |     | kHz   |
| Watchdog timer   | t <sub>WDT</sub>     | Programmable (Reg05 bit[5:4] = 11)       |     | 160 |     | s     |

**NOTE:**

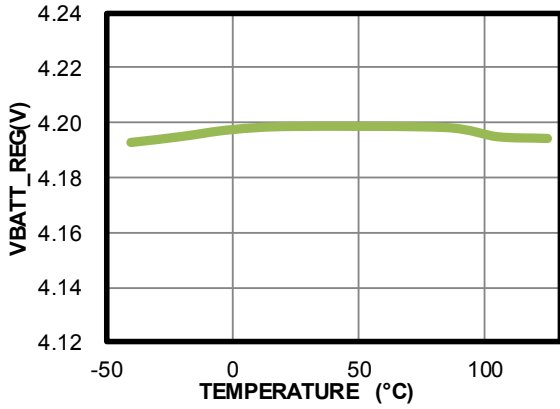
6) Guaranteed by design.

### TYPICAL PERFORMANCE CHARACTERISTICS

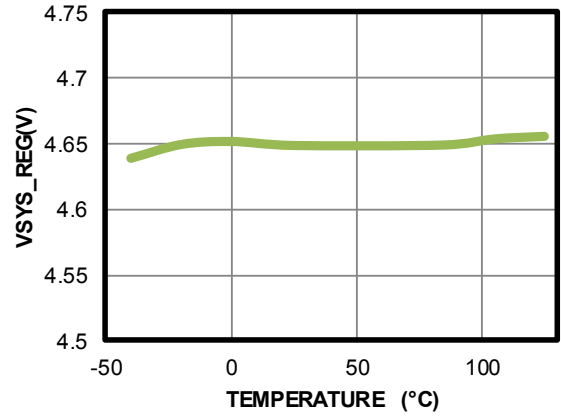
V<sub>IN</sub> = 5V, T<sub>A</sub> = 25°C, I<sub>IN\_LIM</sub> = 455mA, I<sub>CC</sub> = 246mA, V<sub>IN\_MIN</sub> = 4.6V, unless otherwise noted.

**Battery Regulation Voltage vs. Temperature**

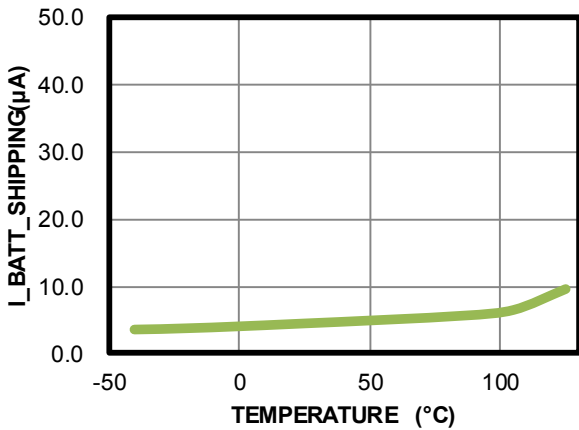
V<sub>BATT\_REG</sub> = 4.2V



**System Regulation Voltage vs. Temperature**

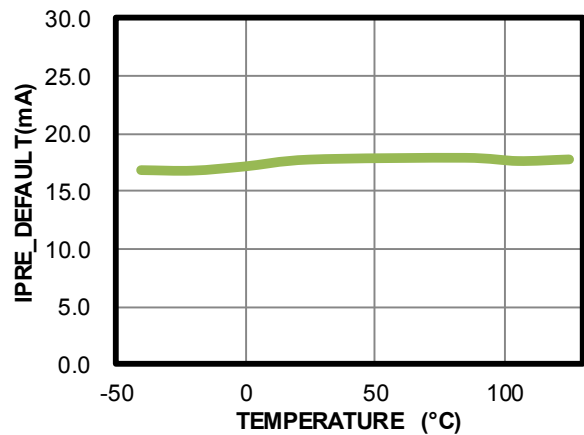


**Battery Current under Shipping Mode vs. Temperature**



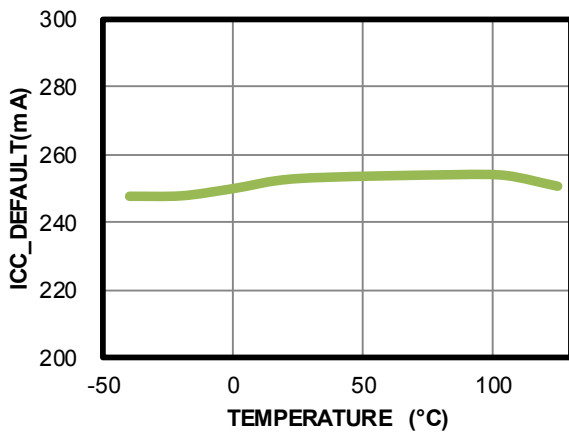
**Pre-Charge Current vs. Temperature**

I<sub>PRE</sub> = 20mA



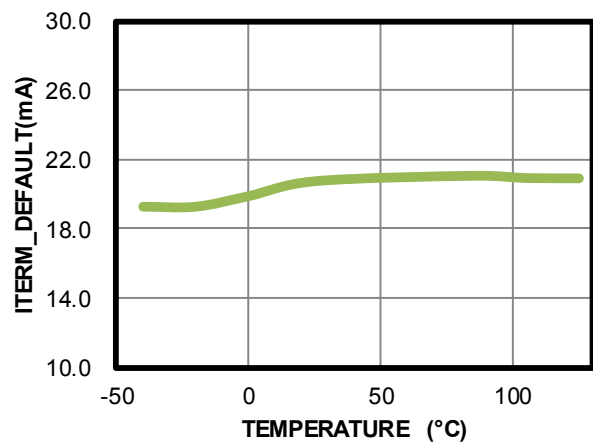
**CC Charge Current vs. Temperature**

I<sub>CC</sub> = 246mA



**Battery Termination Current vs. Temperature**

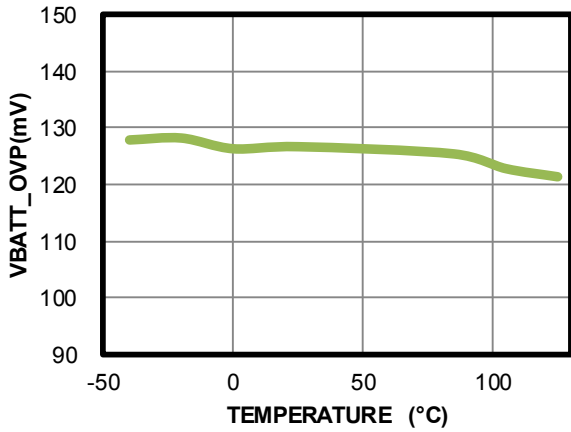
I<sub>TERM</sub> = 20mA



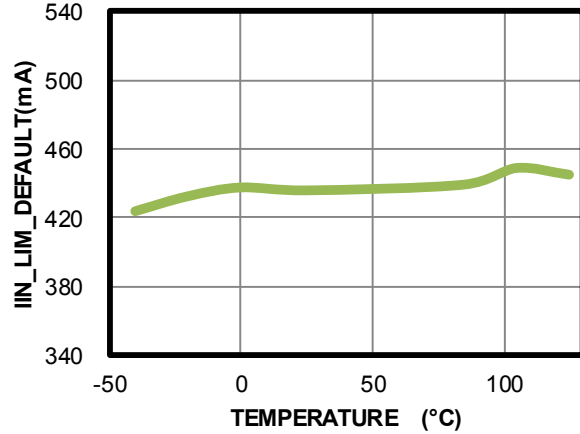
**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

V<sub>IN</sub> = 5V, T<sub>A</sub> = 25°C, I<sub>IN\_LIM</sub> = 455mA, I<sub>CC</sub> = 246mA, V<sub>IN\_MIN</sub> = 4.6V, unless otherwise noted.

**Battery OVP Voltage vs. Temperature**  
Higher than V<sub>BATT\_REG</sub>

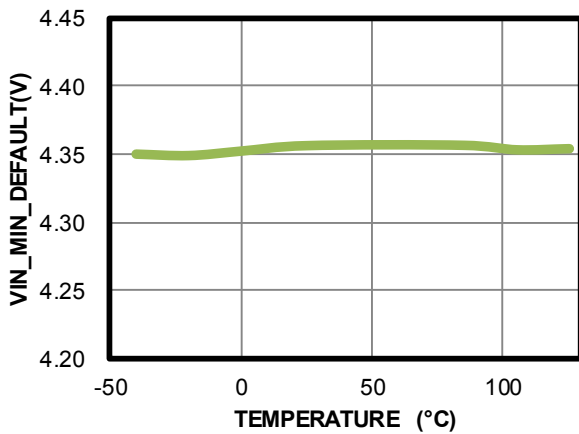


**Input Current Limit vs. Temperature**  
I<sub>IN\_LIM</sub> = 455mA

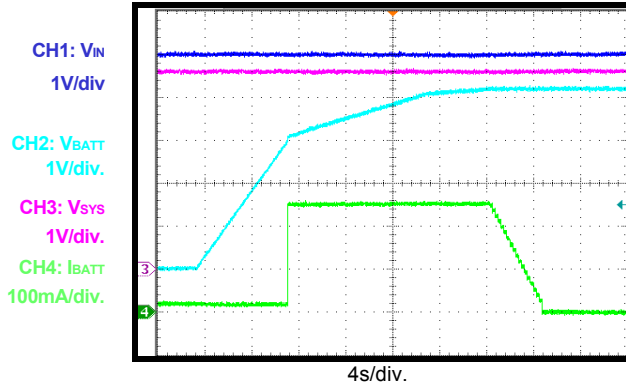
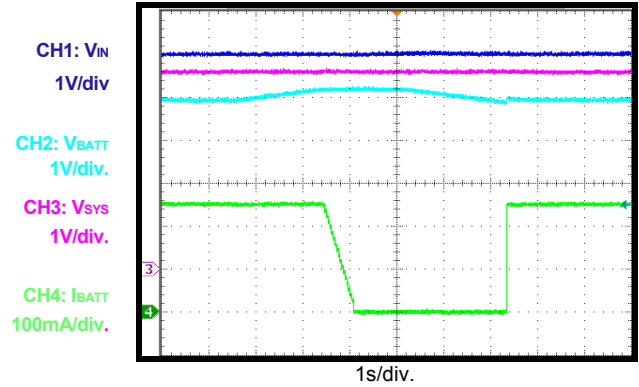
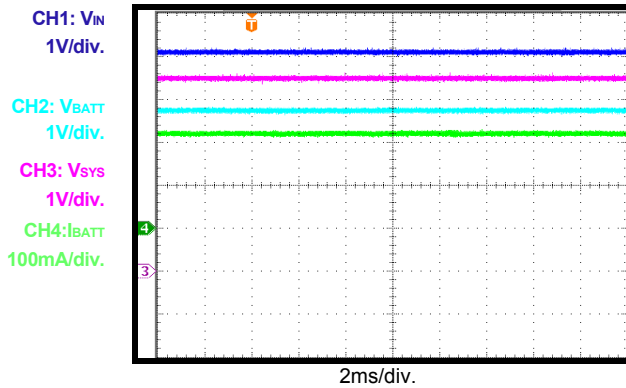
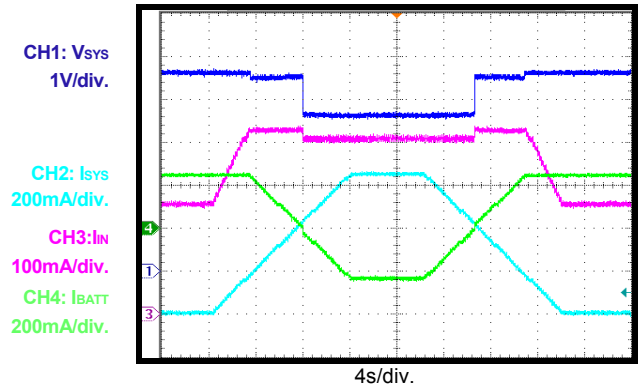
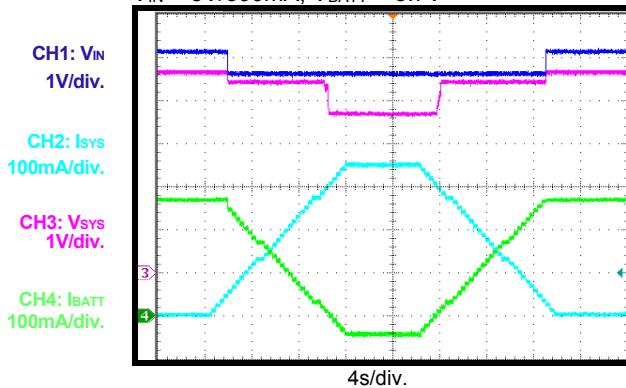
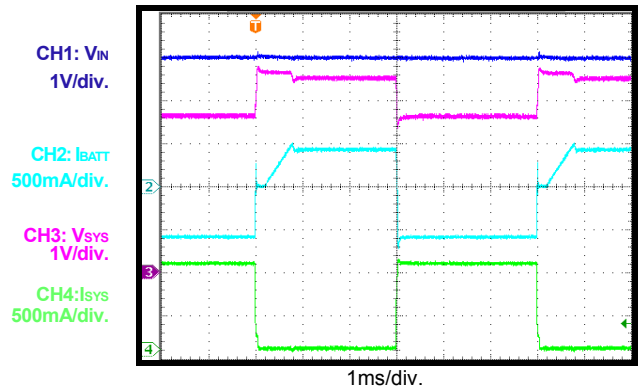


**Input Minimum Voltage vs. Temperature**

V<sub>IN\_MIN</sub> = 4.36V



**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**
 $V_{IN} = 5V$ ,  $T_A = 25^\circ C$ ,  $I_{IN\_LIM} = 455mA$ ,  $I_{CC} = 246mA$ ,  $V_{IN\_MIN} = 4.6V$ , unless otherwise noted.

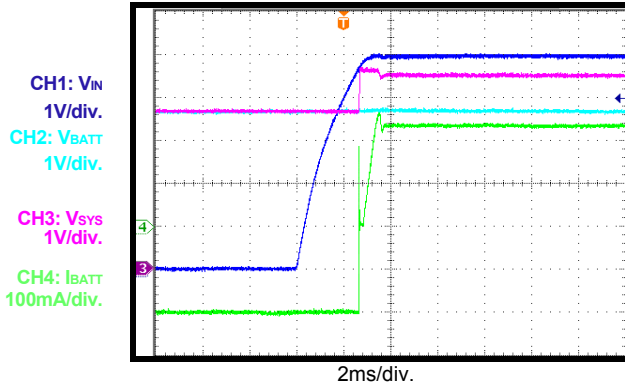
**Battery Charge Curve**
 $I_{SYS} = 0A$ 

**Auto-Recharge**
 $I_{SYS} = 0A$ 

**CC Charge Steady State**
 $V_{BATT} = 3.7V$ ,  $I_{SYS} = 200mA$ 

**Input Current Limit-Based PPM**
 $V_{BATT} = 3.7V$ 

**Input Voltage Regulation-Based PPM**
 $V_{IN} = 5V/300mA$ ,  $V_{BATT} = 3.7V$ 

**SYS Load Transient**
 $V_{IN} = 5V$ ,  $V_{BATT} = 3.7V$ ,  $I_{CC} = 535mA$ ,  $I_{SYS} = 0 - 1A$ 


**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

V<sub>IN</sub> = 5V, T<sub>A</sub> = 25°C, I<sub>IN\_LIM</sub> = 455mA, I<sub>CC</sub> = 246mA, V<sub>IN\_MIN</sub> = 4.6V, unless otherwise noted.

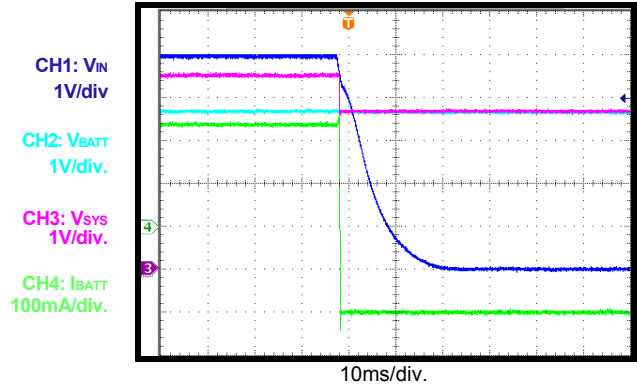
**Power On**

V<sub>BATT</sub> = 3.7V, I<sub>SYS</sub> = 200mA



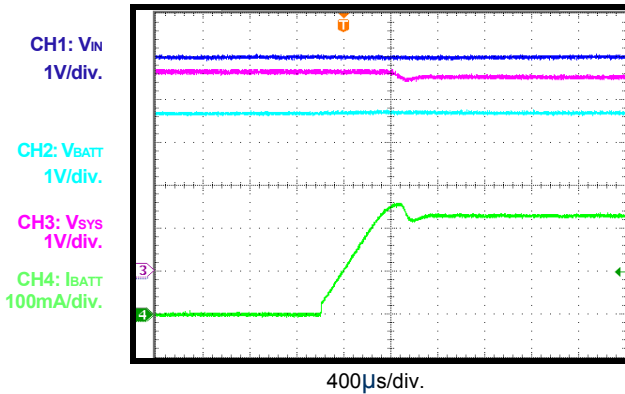
**Power Off**

V<sub>BATT</sub> = 3.7V, I<sub>SYS</sub> = 200mA



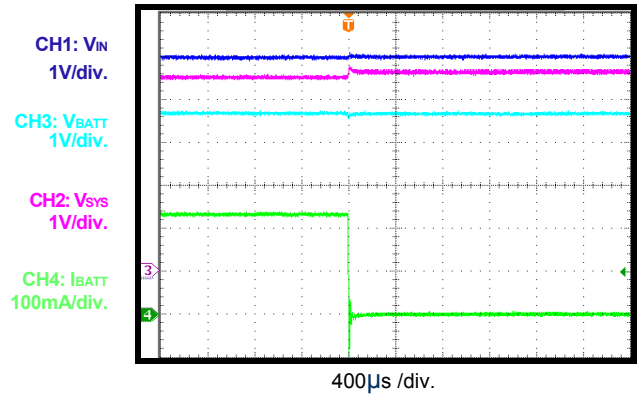
**Charge Enable**

V<sub>BATT</sub> = 3.7V, I<sub>SYS</sub> = 200mA



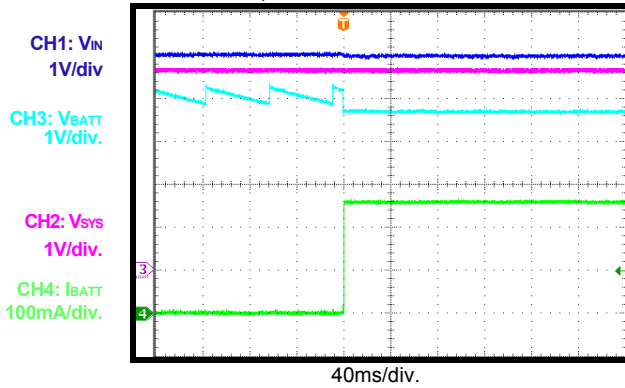
**Charge Disable**

V<sub>BATT</sub> = 3.7V, I<sub>SYS</sub> = 200mA



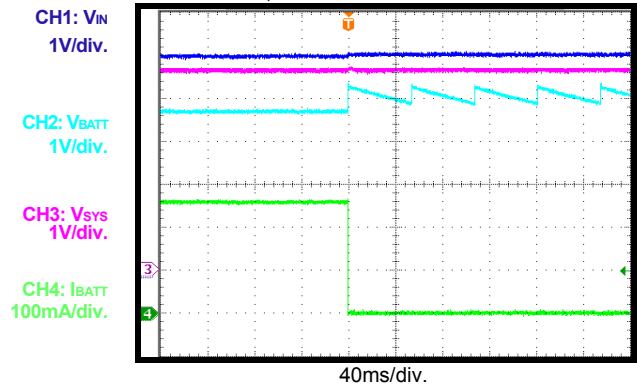
**BATT Insertion**

V<sub>BATT</sub> = 3.7V, I<sub>SYS</sub> = 0A



**BATT Removal**

V<sub>BATT</sub> = 3.7V, I<sub>SYS</sub> = 0A

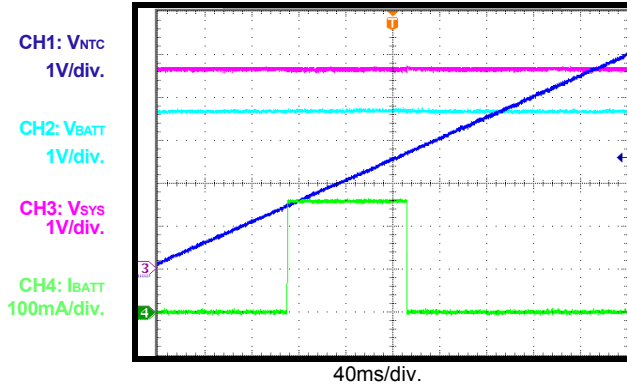


**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

V<sub>IN</sub> = 5V, T<sub>A</sub> = 25°C, I<sub>IN\_LIM</sub> = 455mA, I<sub>CC</sub> = 246mA, V<sub>IN\_MIN</sub> = 4.6V, unless otherwise noted.

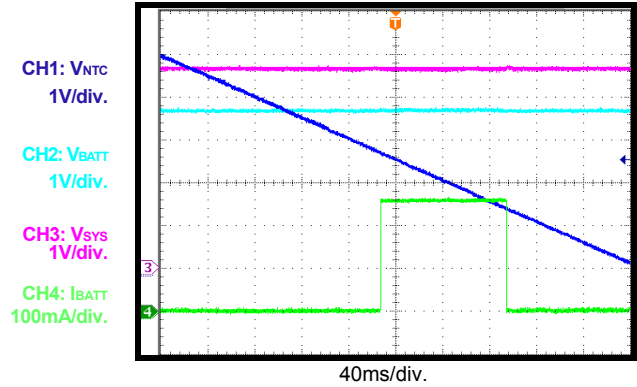
**NTC Rising**

V<sub>BATT</sub> = 3.7V, I<sub>SYS</sub> = 0A, PCB OTP disable



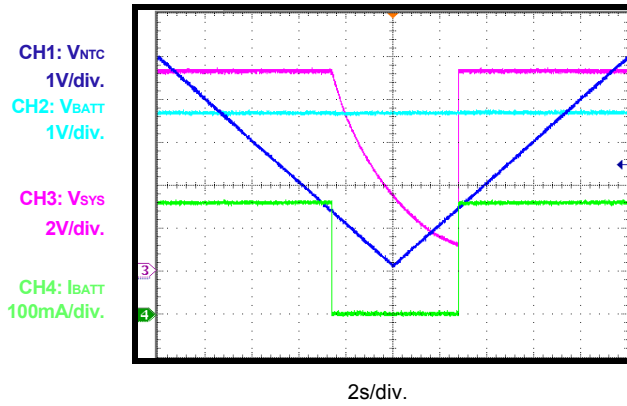
**NTC Falling**

V<sub>BATT</sub> = 3.7V, I<sub>SYS</sub> = 0A, PCB OTP disable



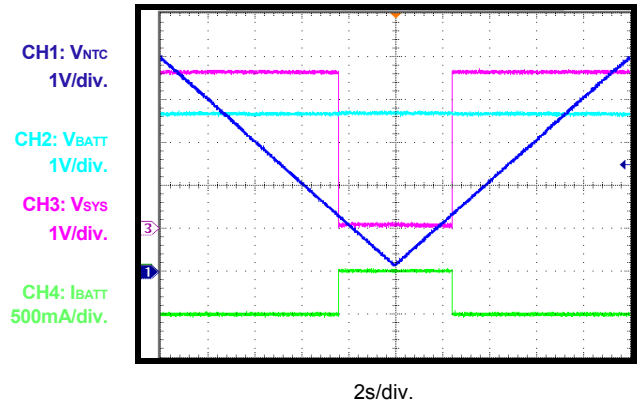
**PCB OTP @ Charge Mode**

V<sub>BATT</sub> = 3.7V, I<sub>SYS</sub> = 0A



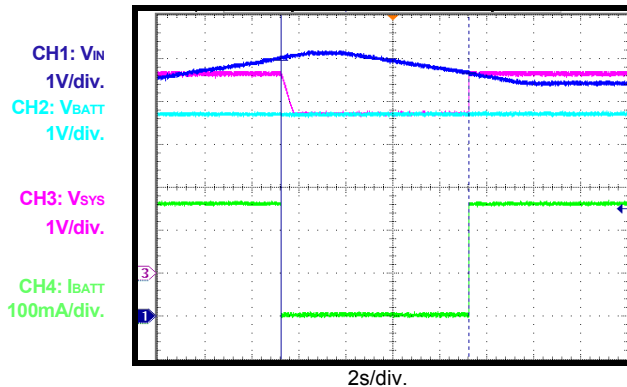
**PCB OTP @ Discharge Mode**

V<sub>IN</sub> = 0V, V<sub>BATT</sub> = 3.7V, I<sub>SYS</sub> = 500mA



**V<sub>IN</sub> OVP Operation**

V<sub>BATT</sub> = 3.7V, I<sub>SYS</sub> = 0A



### BLOCK DIAGRAM

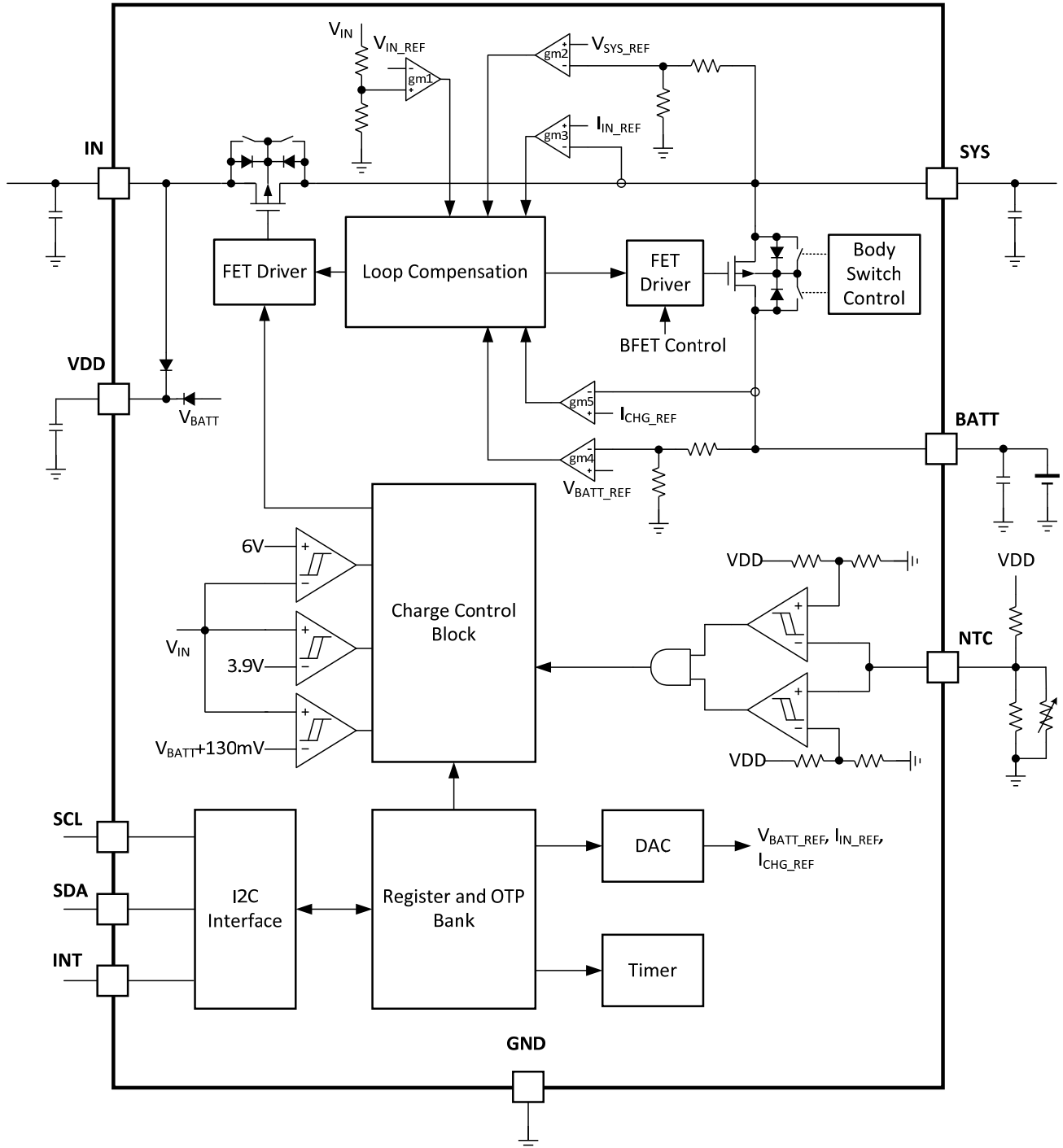


Figure 1: Function Block Diagram

## OPERATION

The MP2664 is an I<sup>2</sup>C-controlled, single-cell, Li-ion or Li-polymer battery charger with complete power path management. The full-charge function features constant current pre-charge (PRE.C), constant current fast-charge (CC) and constant voltage (CV) regulation, charge termination, auto-recharge, and a built-in timer. The power path function allows the input source to power the system and charge the battery simultaneously. If there is a conflict in meeting both the system load and battery charging current, the IC reduces the charging current automatically or uses the battery as a supplemental power to satisfy the system load.

The IC integrates a 300mΩ LDO MOSFET between IN and SYS and a 100mΩ battery MOSFET between SYS and BATT.

In charging mode, the on-chip 100mΩ battery MOSFET works as a full-featured linear charger with constant current pre-charging, constant current fast-charging and constant-voltage charging, charge termination, auto-recharging, NTC monitoring, built-in timer control, and thermal protection. The charge current can be programmed via the I<sup>2</sup>C interface. The IC limits the charge current when the die temperature exceeds the thermal regulation threshold (120°C default).

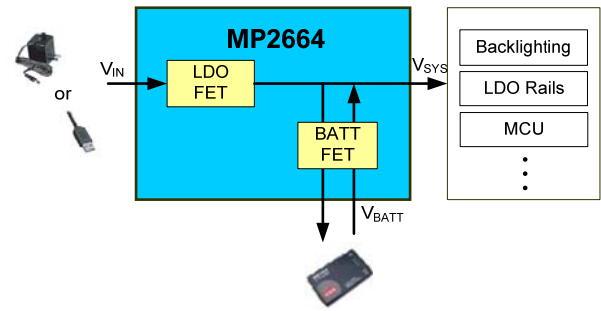
In supplement mode, the 100mΩ battery MOSFET is fully turned on to connect the battery to the system load when the input power is not enough to power the system load. When the input is removed, the 100mΩ battery MOSFET is also fully turned on, allowing the battery to power the system.

When the system load is satisfied, the remaining current is used to charge the smart power path management battery. The IC reduces the charging current or uses power from the battery to satisfy the system load when its demand is over the input power capacity.

Figure 2 shows the power path management structure of the MP2664.

### Power Path Management

The IC employs a direct power path structure with the battery MOSFET decoupling the



**Figure 2: Power Path Management Structure**

### Power Supply

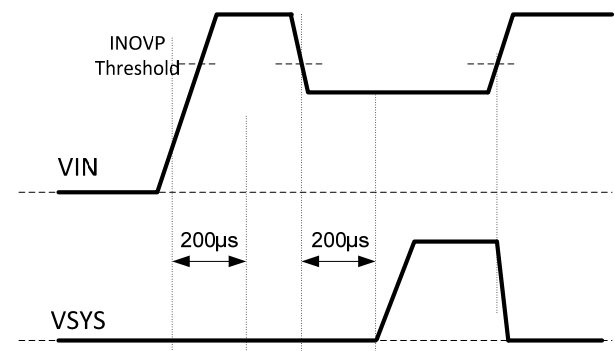
The internal bias circuit of the IC is powered from the higher voltage of IN or BATT. When IN or BATT rises above the respective under-voltage lockout (UVLO) threshold, the sleep comparator, battery depletion comparator, and the battery MOSFET driver are active. The I<sup>2</sup>C interface is ready for communication, and all registers are reset to the default value. The host can access all registers.

### Input OVP and UVLO

The MP2664 has an input over-voltage protection (OVP) threshold and an input UVLO threshold. Once the input voltage exits the normal input voltage range, the Q1 MOSFET is turned off immediately.

When the input voltage is identified as a good source, a 200μs immunity timer becomes active. If the input power is still sufficient until the 200μs timer expires, the system starts up. Otherwise, Q1 remains off.

Figure 3 depicts the operation profile.



**Figure 3: Input Power Detection Operation Profile**

system from the battery, which allows for separate control between the system and the battery. The system is given priority to start up



even with a deeply discharged or missing battery. When the input power is available, even with a depleted battery, the system voltage is always regulated to  $V_{SYS\_REG}$  by the integrated LDO MOSFET.

As shown in Figure 2, the direct power structure is composed of a front-end LDO MOSFET between IN and SYS and a battery MOSFET between SYS and BATT. The LDO MOSFET and battery MOSFET can be controlled by I<sup>2</sup>C.

**Table 1: MOSFET Control by I<sup>2</sup>C**

| MOSFET On/Off Changed By Control | Hi-Z Mode and Charge Control |              |
|----------------------------------|------------------------------|--------------|
|                                  | Set EN_HIZ to 1              | Set CEB to 1 |
| LDO FET                          | OFF                          | x            |
| Battery FET (charging)           | x                            | OFF          |
| Battery FET (discharging)        | x                            | x            |

**NOTE:** x indicates that the value does not matter.

The input LDO (using an LDO MOSFET) provides power to the system, which drives the system load directly and charges the battery through the battery MOSFET.

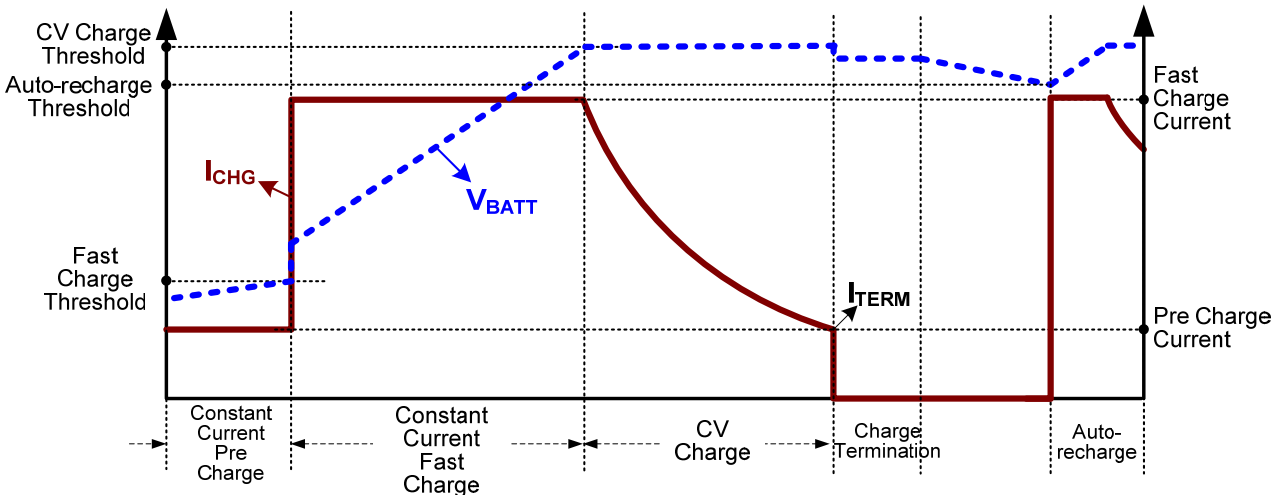
For the system voltage control, when the input voltage is higher than  $V_{SYS\_REG}$ , the system voltage is regulated to  $V_{SYS\_REG}$ . When the input

voltage is lower than  $V_{SYS\_REG}$ , the LDO MOSFET is fully on with the input current limit.

### Battery Charge Profile

The IC provides three main charging phases: constant current pre-charge, constant current fast-charge, and constant-voltage charge (see Figure 4).

1. Phase 1 (constant current pre-charge): The IC is able to pre-charge the deeply depleted battery safely until the battery voltage reaches the pre-charge to the fast-charge threshold ( $V_{BATT\_PRE}$ ). The pre-charge current is programmable via Reg03 bit[1:0]. If  $V_{BATT\_PRE}$  is not reached before the pre-charge timer (1hr) expires, the charge cycle is stopped, and a corresponding timeout fault signal is asserted.
2. Phase 2 (constant current fast charge): When the battery voltage exceeds  $V_{BATT\_PRE}$ , the IC enters a constant current fast-charge phase. The fast-charge current can be programmable via Reg02 bit[4:0].
3. Phase 3 (constant-voltage charge): When the battery voltage rises to the pre-programmable charge full voltage ( $V_{BATT\_REG}$ ) set via Reg04 bit[7:2], the charge mode changes from CC mode to CV mode, and the charge current begins to taper off.



**Figure 4: Battery Charge Profile**

Assuming that the termination function (EN\_TERM) is set via Reg05 bit[6] = 1, the charge cycle is considered to be complete when the following conditions are valid:

- The charge current ( $I_{CHG}$ ) reaches the end of charge (EOC) current threshold ( $I_{TERM}$ ), and the 2.5ms delay timer is initiated.
- During the 2.5ms delay period,  $I_{BATT}$  is always smaller than  $I_{TERM} + I_{TERM\_HYS}$ .

The charge status is marked as complete once the 2.5ms delay timer expires.

The charge current is terminated at the same time if TERM\_TMR is set via Reg05 [0] = 0; otherwise, the charge current continues tapering off.

If EN\_TERM = 0, the termination function is disabled, and the above actions will not occur (see Table 2).

**Table 2: Termination Function Selection Table**

| EN_TERM | TERM_TMR | After $I_{BATT}$ hit $I_{TERM}$ in CV mode |               |
|---------|----------|--|---------------|
|         |          | Operation                                  | Charge Status |
| 0       | x        | Keep CV charge                             | Charge        |
| 1       | 0        | Charge done                                | Charge done   |
| 1       | 1        | Keep CV charge                             | Charge done   |

**NOTE:** x indicates that the value does not matter.

During the charging process, the actual charge current may be less than the register setting due to other loop regulations, such as dynamic power management (DPM) regulation (input voltage, input current) or thermal regulation. If the input current or the input voltage reach their limits during the CV charge, the charge-full termination is not influenced when the charge current is not as close to the EOC current specification.

A new charge cycle starts when the following conditions are valid:

- The input power is recycled
- Battery charging is enabled by the I<sup>2</sup>C
- Auto-recharge kicks in

Under the following conditions:

- No thermistor fault at NTC
- No safety timer fault
- No battery over-voltage
- BATT FET is not forced to turn off

### Automatic Recharge

When the battery is fully charged and the charging is terminated, the battery may be discharged due to system consumption or self-discharge. When the battery voltage is discharged below the recharge threshold and  $V_{IN}$  is still in the operation range, the IC begins another new charging cycle automatically without having to restart the charging cycle manually.

The auto-recharge function is valid only when EN\_TERM = 1 and TERM\_TMR = 0.

### Battery Over-Voltage Protection (OVP)

The IC is designed with a built-in battery over-voltage limit about 130mV higher than  $V_{BATT\_REG}$ . When a battery over-voltage event occurs, the IC suspends the charging immediately and asserts a fault.

### Input Current and Input Voltage-Based Power Management

To meet the input source (usually USB) maximum current-limit specification, the IC uses input current-based power management by monitoring the input current continuously. The total input current limit can be programmed via the I<sup>2</sup>C to prevent the input source from overloading.

If the pre-set input current limit is higher than the rating of the input source, back-up input voltage-based power management also works to prevent the input source from being overloaded. If either the input current limit or the input voltage limit is reached, the Q1 MOSFET between IN and SYS are regulated so that the total input power is limited. As a result, the system voltage drops. Once the system declines to the minimum value of 4.56V or  $V_{IN} - 160mV$ , the charge current is reduced to prevent the system voltage from dropping further.

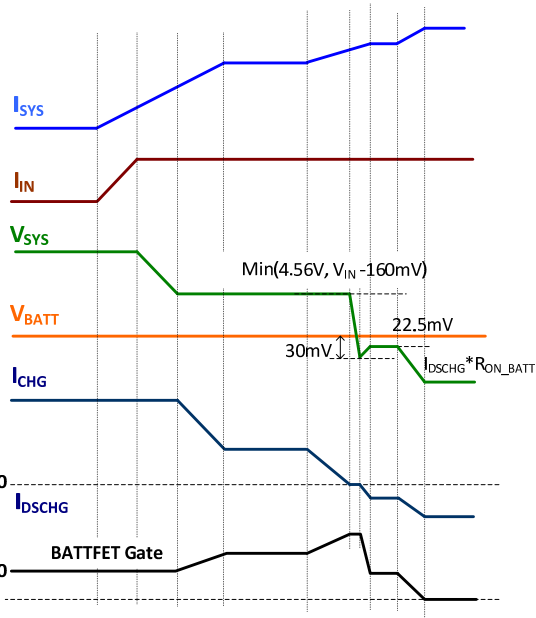
Voltage-based DPM regulates the input voltage to  $V_{IN\_MIN}$  when the load is over the input power capacity.  $V_{IN\_MIN}$  set via the I<sup>2</sup>C should be at least 400mV higher than  $V_{BATT\_REG}$  to ensure the stable operation of the regulator.

### Battery Supplement Mode

The charge current is reduced to keep the input current or input voltage in regulation when DPM occurs. If the charge current is at zero, and the input source is still overloaded due to a heavy system load, the system voltage starts to fall off. Once the system voltage falls below the battery voltage, the IC enters battery supplement mode. When the system voltage is 30mV below the battery voltage, ideal diode mode is enabled. The battery MOSFET is regulated to maintain  $V_{BATT} - V_{SYS}$  at 22.5mV. If the supplement current  $I_{DSCHG} * R_{ON\_BATT}$  is higher than 22.5mV, the battery MOSFET is fully turned on to keep the ideal forward voltage. When the system load decreases, once  $V_{SYS}$  is higher than  $V_{BATT} + 20mV$ , ideal diode mode is disabled.

Figure 5 shows the dynamic power management and battery supplement mode operation profile.

When  $V_{IN}$  is not available, the IC operates in discharge mode, and the battery MOSFET is always fully on to reduce loss.



**Figure 5: Dynamic Power Management and Battery Supplement Operation Profile**

### Battery Regulation Voltage

The battery voltage for the constant-voltage regulation phase is  $V_{BATT\_REG}$ . When  $V_{BATT\_REG}$  is 4.2V, it has a  $\pm 0.5\%$  accuracy over the ambient temperature range of 0°C to +50°C. When the battery is removed, the BATT voltage is between  $V_{BATT\_REG} - V_{RECH}$  and  $V_{BATT\_REG}$ .

### Thermal Regulation and Thermal Shutdown

The IC monitors the internal junction temperature continuously to maximize power delivery and prevent the chip from overheating. When the internal junction temperature reaches the pre-set limit of  $T_{J\_REG}$  (default 120°C), the IC reduces the charge current to prevent higher power dissipation. The multiple thermal regulation thresholds from 60°C to 120°C help the system design meet the thermal requirement in different applications. The junction temperature regulation threshold can be set via Reg06 bit[1:0].

When the junction temperature reaches 150°C, both Q1 and Q2 are turned off.

### Negative Temperature Coefficient (NTC) Temperature Sensor

NTC allows the IC to sense the battery temperature using the thermistor usually available in the battery pack to ensure a safe operating environment for the chip. A resistor with an appropriate value should be connected from VDD to NTC, and the thermistor should be connected from NTC to ground. The voltage on NTC is determined by the resistor divider, whose divide ratio depends on the temperature. The IC sets a pre-determined upper and lower bound of the divide ratio internally for NTC cold and NTC hot. In the MP2664, the I<sup>2</sup>C default setting is the PCB OTP. The function can be changed through the I<sup>2</sup>C (see Table 3).

**Table 3: NTC Function Selection Table**

| I <sup>2</sup> C Control |            | Function |
|--------------------------|------------|----------|
| EN_NTC                   | EN_PCB OTP |          |
| 0                        | x          | Disable  |
| 1                        | 1          | NTC      |
| 1                        | 0          | PCB OTP  |

When PCB OTP is selected, if the NTC voltage is lower than the NTC hot threshold, both the LDO MOSFET and battery MOSFET are off. The PCB OTP fault sets the NTC\_FAULT status (Reg08 bit[1]) to 1 to indicate the fault. Operation resumes once the NTC voltage is higher than the NTC hot threshold.

The NTC function only works in charge mode. Once the NTC voltage goes out of the divide ratio (the temperature is outside the safe operating range), the IC stops the charging and reports it on the status bits. Charging resumes automatically after the temperature falls back to the safe range.

### Safety Timer

The IC provides both a pre-charge and a fast-charge safety timer to prevent extended charging cycles due to abnormal battery conditions. The safety timer is one hour when the battery voltage is below  $V_{BATT\_PRE}$ . The fast-charge safety timer begins when the battery enters constant current fast charging. The fast-charge safety timer can be programmed through the I<sup>2</sup>C. The safety timer feature can be disabled via the I<sup>2</sup>C.

The following actions can restart the safety timer:

- A new charge cycle is kicked in
- Reg01 bit[3] is written from 0 to 1 (charge enable)
- Reg05 bit[3] is written from 0 to 1 (safety timer enable)
- Reg01 bit[7] is written from 0 to 1 (software reset)

### Host Mode and Default Mode

The IC is a host-controlled device. After the power-on reset, the IC starts in the watchdog timer expiration state or default mode. All of the registers are in the default settings.

Any write to the IC changes it to host mode. All charge parameters are programmable. If the watchdog timer (Reg05 bit[5:4]) is not disabled, the host must reset the watchdog timer regularly by writing 1 to the Reg01 bit[6] before the watchdog timer expires to keep the device in host mode. Once the watchdog timer expires, the IC returns to default mode. The watchdog timer limit can also be programmed or disabled

by the host control. When there is no  $V_{IN}$ , the watchdog timer is suspended (see Figure 10).

The operation can also be changed to default mode when one of the following conditions occur:

- Refresh input without battery
- Re-insert battery with no  $V_{IN}$
- Register reset Reg01 bit[7] is reset

### Battery Discharge Function

If battery is connected and the input source is missing, the battery MOSFET is fully on when  $V_{BATT}$  is above the  $V_{BATT\_UVLO}$  threshold. The 100mΩ battery MOSFET minimizes conduction loss during discharge. The quiescent current of the IC is as low as 11μA in this mode. The low on resistance and low quiescent current help extend the running time of the battery.

### Over-Discharge Current Protection

The IC has an over-discharge current protection in discharge mode and supplement mode. Once  $I_{BATT}$  exceeds the programmable discharge current limit (default 1.785A), the battery MOSFET is turned off after a 60μs delay, and the MP2664 enters hiccup mode in over-current protection (OCP). The discharge current can be programmed high to 3.2A through the I<sup>2</sup>C. If the discharge current goes high to reach the internal fixed current limit (about 3.7A), the battery MOSFET is turned off and starts hiccup mode immediately.

Similarly, when the battery voltage falls below the programmable  $V_{BATT\_UVLO}$  threshold (default 2.8V), the battery MOSFET is turned off to prevent over-discharge.

### System Short-Circuit Protection (SCP)

The MP2664 features SYS node short-circuit protection (SCP) for the IN to SYS path and the BATT to SYS path.

The system voltage is monitored continuously. If  $V_{SYS}$  is lower than 1.5V, the system (SCP) for the IN to SYS path and the BATT to SYS path are active.  $I_{DSCHG}$  is decreased to half of the original value.

- 1) IN to SYS path: Once  $I_{IN}$  is over the protection threshold, both the LDO MOSFET and the BATT MOSFET are turned off immediately, and the IC enters hiccup mode. Otherwise, the max current limit and the setting input current limit are not reached, and  $I_{IN}$  is regulated at  $I_{IN\_LIM}$ . Hiccup mode also starts after a 60 $\mu$ s delay. The interval of the hiccup mode is 800 $\mu$ s.
- 2) BATT to SYS path: Once  $I_{BATT}$  is over the 3.7A protection threshold, both the LDO MOSFET and the BATT MOSFET are turned off immediately, and the IC enters hiccup mode. When the battery discharge current limit threshold is reached, hiccup mode starts after a 60 $\mu$ s delay. The interval of the hiccup mode is 800 $\mu$ s.

If a system short-circuit occurs when both the input and battery are present, the protection mechanism of both paths work, with the faster one dominating the hiccup operation (see Figure 13).

### Interrupt to Host (INT)

The IC has an alert mechanism that can output an interrupt signal via INT to notify the system of the operation by outputting a 256 $\mu$ s low-state INT pulse. Any of the below events can trigger the INT output:

- Good input source detected
- UVLO or input over-voltage protection (OVP) charge completed
- Charging status change
- Any fault in Reg08 (watchdog timer fault, input fault, thermal fault, safety timer fault, battery OVP fault, NTC fault)

When any fault occurs, the IC sends out an INT pulse and latches the fault state in Reg08. After the IC exits the fault state, the fault bit can be released to 0 after the host reads Reg08. The NTC fault is not latched and always reports the current thermistor conditions.

Note that the INT needs the external pull-up resistor for its open-drain connection. The resistance should not be lower than 200k $\Omega$ .

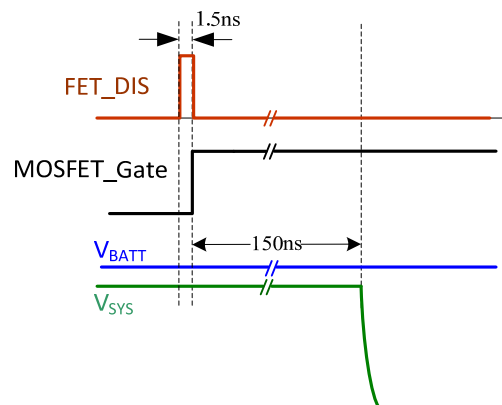
### Battery Disconnect Function

In applications where the battery is not removable, it is essential to disconnect the battery from the system for two reasons: to prevent excessive capacity discharge when the device is in shipping or storage mode, and to allow the system power to reset.

The MP2664 provides both shipping mode and system reset mode for different application requirements.

The register bit FET\_DIS (Reg06 bit[5]), allows the IC to enter shipping mode. During normal operation, the battery MOSFET is turned on, and this bit is 0. If this bit is set to 1 through the I<sup>2</sup>C, the battery MOSFET is turned off, and the MP2664 enters shipping mode. The FET\_DIS bit is reset to 0 automatically after the battery MOSFET is turned off (see Figure 6).

The IC can exit shipping mode by pulling INT down. When the IC is in shipping mode and only the battery is present, pull INT down by pushing the push button (PB) to wake the MP2664 up from shipping mode (see Table 4).



**Figure 6: Time Delay from when FET\_DIS is written to 1 to the Battery MOSFET Turning Off**



**Table 4: Exit the Shipping Mode with BATT Present Only**

|        | INT Signal                                  | IC Exits Shipping Mode |
|--------|---|------------------------|
| Case 1 | INT = low twice with the rising edge >600ns | At once                |
| Case 2 | INT = low once with the rising edge >600ns  | After 4s               |
| Case 3 | INT = low for 4s                            | After 4s               |
| Case 4 | INT = low with the rising edge in ms level  | At once                |

The MP2664 can also wake up from shipping mode when a valid  $V_{IN}$  powers on (see Table 5). After  $V_{IN}$  is preset, the MP2664 pulls INT low to indicate the event "Good input source detected" if  $V_{IN}$  is in the operating range. Then, the MP2664 can be woken up from shipping mode by the INT signal (see Figure 7).

**Table 5: Exiting Shipping Mode when  $V_{IN}$  Powers On**

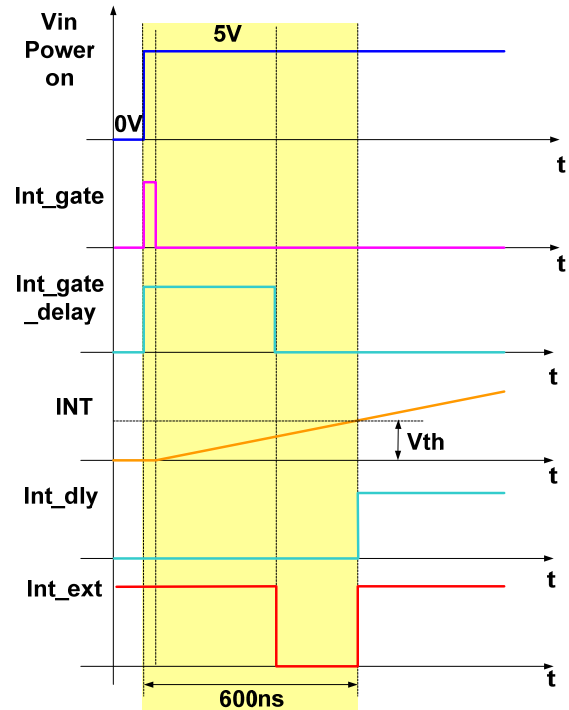
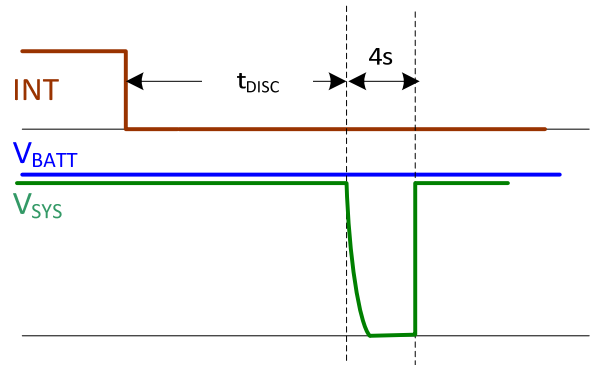
|        | INT Signal                                 | IC Exits Shipping Mode |
|--------|--|------------------------|
| Case 1 | INT= low twice with the rising edge >600ns | At once                |
| Case 2 | INT= low once with the rising edge >600ns  | After 4s               |
| Case 3 | INT = low with the rising edge in ms level | At once                |

If FET\_DIS is set to 1 during shipping mode, the IC can wake up after keeping INT low for 4s. In this case, the FET\_DIS bit cannot be reset to 0 automatically—it must be reset to 0 manually through the I<sup>2</sup>C.

The IC can use INT to cut off the path from the battery to the system when a system reset is needed.

Once the logic at INT is set to low for more than 16s, the battery is disconnected from the system by turning off the battery MOSFET.

The off state lasts for 4s, and then the battery MOSFET is turned on automatically. The system is powered by the battery again. During the 4s off period, the INT pin voltage level can be high or low. The IC can reset the system by controlling INT (see Figure 8).


**Figure 7: INT Signal during  $V_{IN}$  Power On**

**Figure 8: System Reset Function Operation Profile**

## I<sup>2</sup>C REGISTER MAP

IC Address: 09H (reserved some trim options)

### Input Source Control Register/Address: 00H (Default: 0100 1111)

| Bit                              | Symbol                  | Description   | Read/Write | Default  |
|----------------------------------|-------------------------|---|------------|--|
| Bit 7                            | EN_HIZ <sup>(7)</sup>   | 0: disable<br>1: enable   | r/w        | Disable (0)  |
| Input Minimum Voltage Regulation |                         |   |            |  |
| Bit 6                            | V <sub>IN_MIN</sub> [3] | 640mV   | r/w        | Offset: 3.88V<br>Range: 3.88V - 5.08V<br>Default: 4.60V (1001) |
| Bit 5                            | V <sub>IN_MIN</sub> [2] | 320mV   |            |  |
| Bit 4                            | V <sub>IN_MIN</sub> [1] | 160mV   |            |  |
| Bit 3                            | V <sub>IN_MIN</sub> [0] | 80mV  |            |  |
| Input Current Limit              |                         |   |            |  |
| Bit 2                            | I <sub>IN_LIM</sub> [2] | 000: 85mA<br>001: 130mA<br>010: 175mA<br>011: 220mA<br>100: 265mA<br>101: 310mA<br>110: 355mA<br>111: 455mA | r/w        | 455mA (111)  |
| Bit 1                            | I <sub>IN_LIM</sub> [1] |   |            |  |
| Bit 0                            | I <sub>IN_LIM</sub> [0] |   |            |  |

**NOTE:**

7) This bit only controls the on and off of the LDO MOSFET.

### Power-On Configuration Register/Address: 01H (Default: 0000 0100)

| Bit                    | Symbol                                | Description                             | Read/Write | Default   |
|------------------------|---------------------------------------|---|------------|---|
| Bit 7                  | Register reset                        | 0: keep current setting<br>1: reset     | r/w        | Keep current setting (0)                                  |
| Bit 6                  | I <sup>2</sup> C watchdog timer reset | 0: normal<br>1: reset                   | r/w        | Normal (0)  |
| Bit 5                  | Reserved                              |   | r/w        | Reserved  |
| Bit 4                  | Reserved                              |   | r/w        | Reserved  |
| Charger Configuration  |                                       |   |            |   |
| Bit 3                  | CEB                                   | 0: charge enabled<br>1: charge disabled | r/w        | Charge enabled (0)  |
| Battery UVLO Threshold |                                       |   |            |   |
| Bit 2                  | V <sub>BATT_UVLO</sub> [2]            | 0.4V                                    | r/w        | Offset: 2.4V<br>Range: 2.4V - 3.1V<br>Default: 2.8V (100) |
| Bit 1                  | V <sub>BATT_UVLO</sub> [1]            | 0.2V                                    |            |   |
| Bit 0                  | V <sub>BATT_UVLO</sub> [0]            | 0.1V                                    |            |   |

**Charge Current Control Register/Address: 02H (Default: 0000 1110)**

| Bit                         | Symbol              | Description | Read/Write | Default  |
|-----------------------------|---------------------|-------------|------------|--|
| Bit 7                       | Reserved            |             | r/w        | Reserved   |
| Bit 6                       | Reserved            |             | r/w        | Reserved   |
| Bit 5                       | Reserved            |             | r/w        | Reserved   |
| Fast-Charge Current Setting |                     |             |            |  |
| Bit 4                       | I <sub>CC</sub> [4] | 272mA       | r/w        | Offset: 8mA<br>Range: 8mA - 535mA<br><br>Default: 246mA<br>(01110) |
| Bit 3                       | I <sub>CC</sub> [3] | 136mA       |            |  |
| Bit 2                       | I <sub>CC</sub> [2] | 68mA        |            |  |
| Bit 1                       | I <sub>CC</sub> [1] | 34mA        |            |  |
| Bit 0                       | I <sub>CC</sub> [0] | 17mA        |            |  |

**Pre-Charge/Termination Current/Address: 03H (Default: 0100 1010)**

| Bit                                 | Symbol                 | Description             | Read/Write | Default  |
|-------------------------------------|------------------------|-------------------------|------------|--|
| Bit 7                               | Reserved               |                         | r/w        | Reserved   |
| BATT to SYS Discharge Current Limit |                        |                         |            |  |
| Bit 6                               | I <sub>DSCHG</sub> [3] | 1600mA                  | r/w        | Offset: 200mA<br>Range: 400mA - 3.2A<br>Valid range: 0001 - 1111<br>Default: 2000mA<br>(1001)                  |
| Bit 5                               | I <sub>DSCHG</sub> [2] | 800mA                   |            |  |
| Bit 4                               | I <sub>DSCHG</sub> [1] | 400mA                   |            |  |
| Bit 3                               | I <sub>DSCHG</sub> [0] | 200mA                   |            |  |
| PCB OTP Enable                      |                        |                         |            |  |
| Bit 2                               | EN_PCB OTP             | 0: enable<br>1: disable | r/w        | Enable(0)  |
| Pre-Charge Current                  |                        |                         |            |  |
| Bit 1                               | I <sub>PRE</sub> [1]   | 14mA                    | r/w        | Offset: 6mA<br>Range: 6mA - 27mA<br>Default: 20mA (10)<br>I <sub>PRE</sub> [1:0] also sets termination current |
| Bit 0                               | I <sub>PRE</sub> [0]   | 7mA                     |            |  |



**Charge Voltage Control Register/Address: 04H (Default: 1010 0011)**

| Bit   | Symbol                    | Description          | Read/Write | Default  |
|---|---------------------------|----------------------|------------|--|
| Battery Regulation Voltage                                |                           |                      |            |  |
| Bit 7   | V <sub>BATT_REG</sub> [5] | 480mV                | r/w        | Offset: 3.60V<br>Range: 3.60V - 4.545V<br>Default: 4.2V (101000) |
| Bit 6   | V <sub>BATT_REG</sub> [4] | 240mV                |            |  |
| Bit 5   | V <sub>BATT_REG</sub> [3] | 120mV                |            |  |
| Bit 4   | V <sub>BATT_REG</sub> [2] | 60mV                 |            |  |
| Bit 3   | V <sub>BATT_REG</sub> [1] | 30mV                 |            |  |
| Bit 2   | V <sub>BATT_REG</sub> [0] | 15mV                 |            |  |
| Pre-Charge to Fast Charge Threshold                       |                           |                      |            |  |
| Bit 1   | V <sub>BATT_PRE</sub>     | 0: 2.8V<br>1: 3.0V   | r/w        | 3.0V (1)   |
| Battery Recharge Threshold (below V <sub>BATT_REG</sub> ) |                           |                      |            |  |
| Bit 0   | V <sub>RECH</sub>         | 0: 150mV<br>1: 300mV | r/w        | 300mV (1)  |

**Charge Termination/Timer Control Register/Address: 05H (Default: 0100 1010)**

| Bit   | Symbol       | Description   | Read/Write | Default            |
|---|--------------|---|------------|--------------------|
| Bit 7   | Reserved     |   | r/w        | Reserved           |
| Termination Setting (the termination is allowed or not)   |              |   |            |                    |
| Bit 6   | EN_TERM      | 0: disable<br>1: enable                             | r/w        | Enabled (1)        |
| I <sup>2</sup> C Watchdog Timer Limit   |              |   |            |                    |
| Bit 5   | WATCHDOG [1] | 00: disable timer<br>01: 40s<br>10: 80s<br>11: 160s | r/w        | Disable timer (00) |
| Bit 4   | WATCHDOG [0] |   |            |                    |
| Safety Timer Setting  |              |   |            |                    |
| Bit 3   | EN_TIMER     | 0: disable<br>1: enable                             | r/w        | Enable timer (1)   |
| Fast-Charge Timer   |              |   |            |                    |
| Bit 2   | CHG_TMR [1]  | 00: 3hrs<br>01: 5hrs<br>10: 8hrs<br>11: 12hrs       | r/w        | 5hrs (01)          |
| Bit 1   | CHG_TMR [0]  |   |            |                    |
| Termination Timer Control (when TERM_TMR is enabled, the IC will not suspend the charge current after charge termination) |              |   |            |                    |
| Bit 0   | TERM_TMR     | 0: disable<br>1: enable                             | r/w        | (0)                |

**Miscellaneous Operation Control Register/Address: 06H (Default: 0100 1011)**

| Bit                          | Symbol                  | Description                                    | Read/Write | Default                   |
|------------------------------|-------------------------|--|------------|---------------------------|
| Bit 7                        | Reserved                |  | r/w        | Read/write                |
| Bit 6                        | Reserved                |  | r/w        | This bit must be set to 0 |
| Bit 5                        | FET_DIS <sup>(8)</sup>  | 0: enable<br>1: turn off                       | r/w        | Enabled (0)               |
| Bit 4                        | Reserved                |  | r/w        | (0)                       |
| Bit 3                        | EN_NTC                  | 0: disable<br>1: enable                        | r/w        | Enabled (1)               |
| Bit 2                        | Reserved                |  | r/w        |                           |
| Thermal Regulation Threshold |                         |  |            |                           |
| Bit 1                        | T <sub>J</sub> _REG [1] | 00: 60°C<br>01: 80°C<br>10: 100°C<br>11: 120°C | r/w        | 120°C (11)                |
| Bit 0                        | T <sub>J</sub> _REG [0] |  |            |                           |

**NOTE:**

8) This bit controls the on and off of the battery MOSFET, including the charging and discharging.

**System Status Register/Address: 07H (Default: 0000 0000)**

| Bit      | Symbol       | Description   | Read/Write | Default  |
|----------|--------------|---|------------|--|
| Bit 7    | Reserved     |   | r          | Reserved   |
| Revision |              |   |            |  |
| Bit 6    | Rev [1]      | Revision number   | r          | (00)   |
| Bit 5    | Rev [0]      |   |            |  |
| Bit 4    | CHG_STAT [1] | 00: not charging<br>01: pre-charge<br>10: charge<br>11: charge done | r          | Not charging (00)                                |
| Bit 3    | CHG_STAT [0] |   |            |  |
| Bit 2    | PPM_STAT     | 0: no PPM<br>1: in PPM  | r          | No PPM (0)<br>(no power-path management happens) |
| Bit 1    | PG_STAT      | 0: power fail<br>1: power good                                      | r          | Not power good (0)                               |
| Bit 0    | THERM_STAT   | 0: no thermal regulation<br>1: in thermal regulation                | r          | Normal (0)                                       |

**Fault Register/Address: 08H (Default: 0000 0000)**

| Bit   | Symbol         | Description                                     | Read/Write | Default     |
|-------|----------------|---|------------|-------------|
| Bit 7 | Reserved       |   | r          | Reserved    |
| Bit 6 | WATCHDOG_FAULT | 0: normal<br>1: watchdog timer expiration       | r          | Normal (0)  |
| Bit 5 | VIN_FAULT      | 0: normal<br>1: input fault (OVP or bad source) | r          | Normal (00) |
| Bit 4 | THEM_SD        | 0: normal<br>1: thermal shutdown                | r          |             |
| Bit 3 | BAT_FAULT      | 0: normal<br>1: battery OVP                     | r          | Normal (0)  |
| Bit 2 | STMR_FAULT     | 0: normal<br>1: safety timer expiration         | r          | Normal (0)  |
| Bit 1 | NTC_FAULT [1]  | 0: normal<br>1: NTC hot                         | r          | Normal (00) |
| Bit 0 | NTC_FAULT [0]  | 0: normal<br>1: NTC cold                        |            |             |



### OTP MAP

| #    | Bit7  | Bit6 | Bit5     | Bit4                                      | Bit3       | Bit2 | Bit1             | Bit0 |
|------|---|------|----------|---|------------|------|------------------|------|
| 0x02 | N/A   |      |          | I <sub>CC</sub> : 8mA - 535mA / 17mA step |            |      |                  |      |
| 0x03 | N/A   |      |          |   | EN_PCB_OTP |      | I <sub>PRE</sub> |      |
| 0x04 | V <sub>BATT_REG</sub> : 3.6V - 4.545V / 15mV step |      |          |   |            |      |                  | N/A  |
| 0x05 | N/A   |      | WATCHDOG |   | N/A        |      |                  |      |

### OTP DEFAULT

| OTP Items             | Default       |
|-----------------------|---------------|
| I <sub>CC</sub>       | 246mA         |
| I <sub>PRE</sub>      | 20mA          |
| V <sub>BATT_REG</sub> | 4.2V          |
| WATCHDOG              | Disable timer |
| EN_PCB_OTP            | Enable        |

### STATE CONVERSION CHART

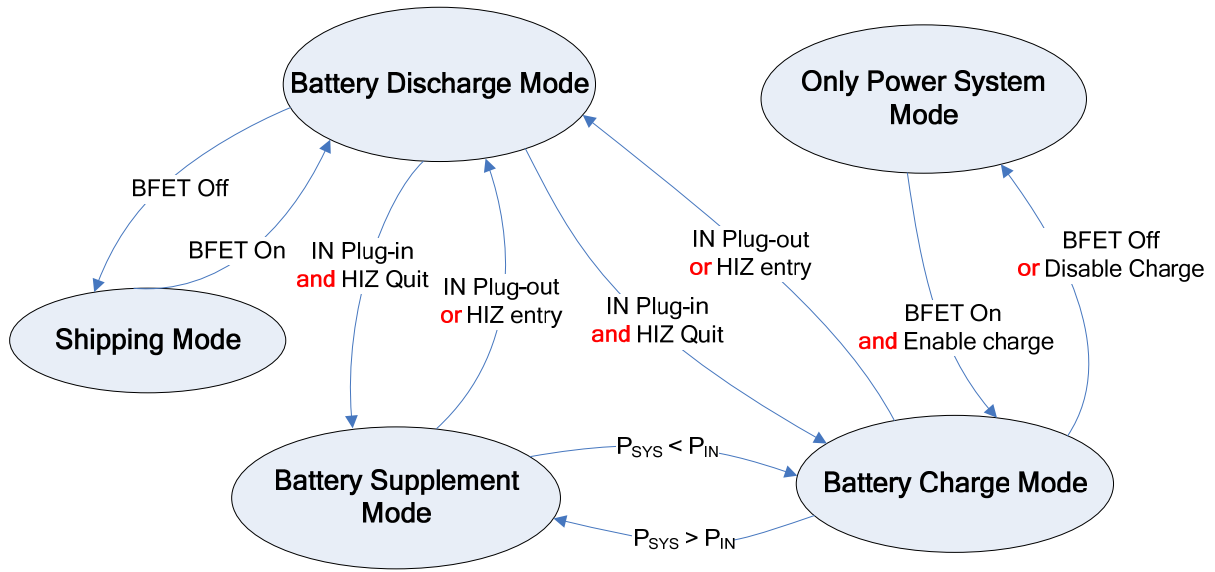


Figure 9: State Machine Conversion

CONTROL FLOW CHART

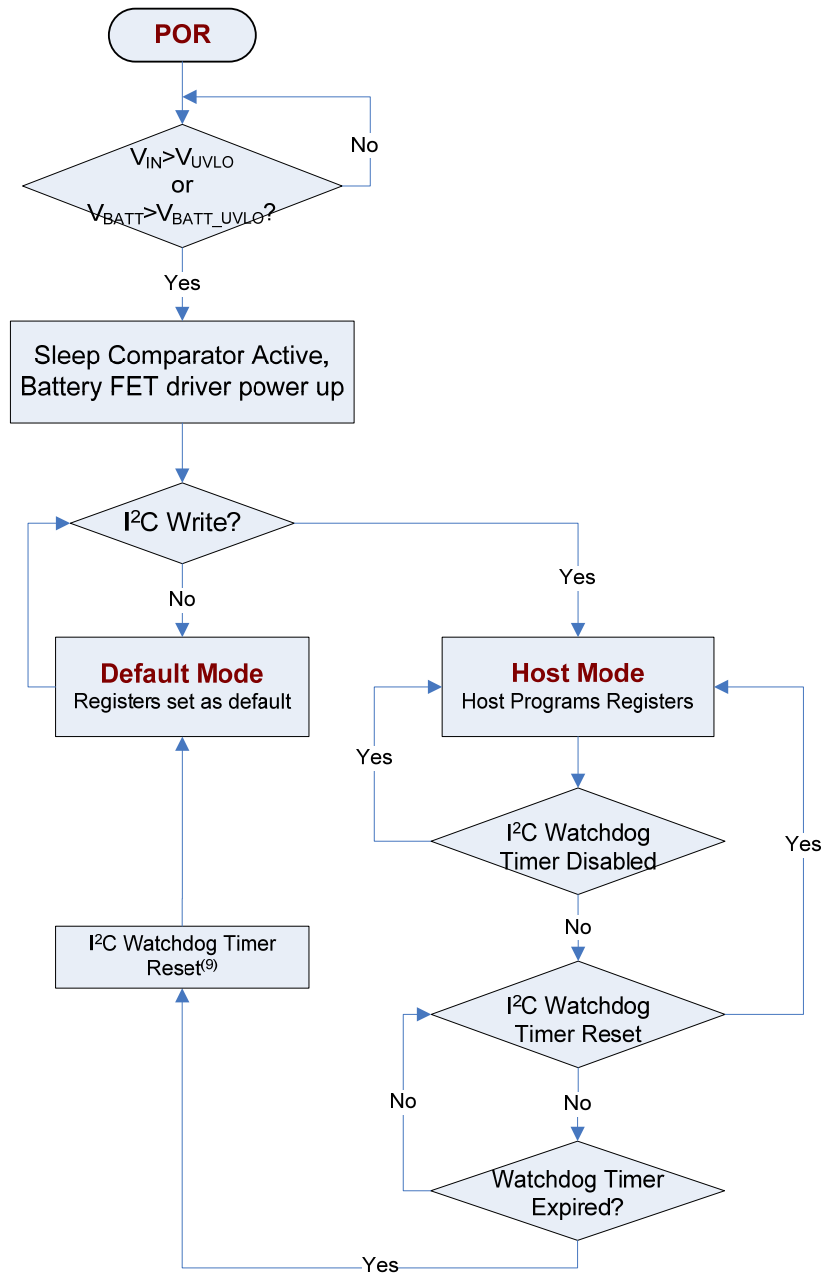


Figure 10: Default Mode and Host Mode Selection <sup>(10)</sup>

NOTES:

- 9) Once the watchdog timer expires, the I<sup>2</sup>C watchdog timer must be reset, or the watchdog timer is not valid in the next cycle.
- 10) The watchdog timer is held when V<sub>IN</sub> is not present.

CONTROL FLOW CHART (continued)

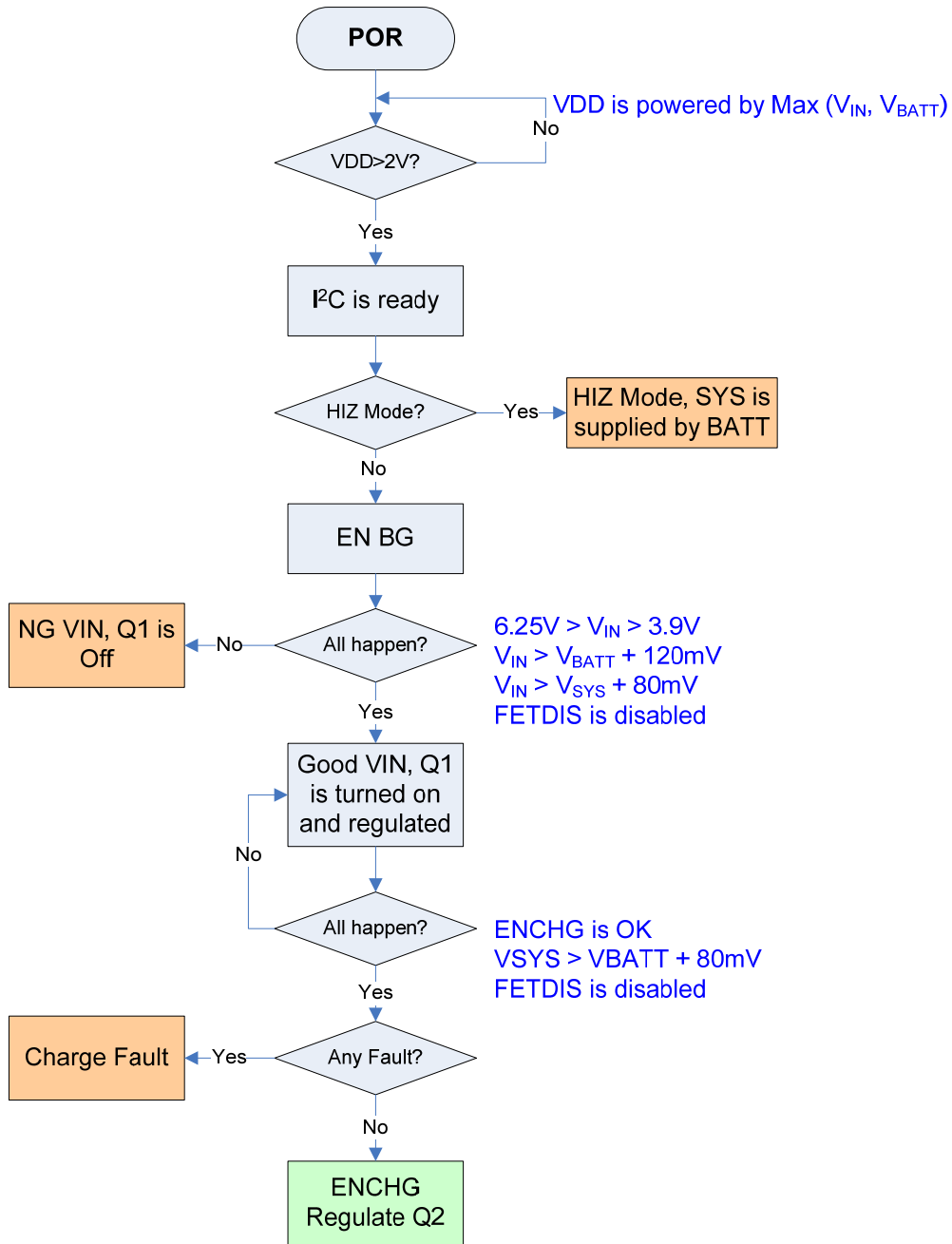


Figure 11: Input Power Start-Up Flow Chart

CONTROL FLOW CHART (continued)

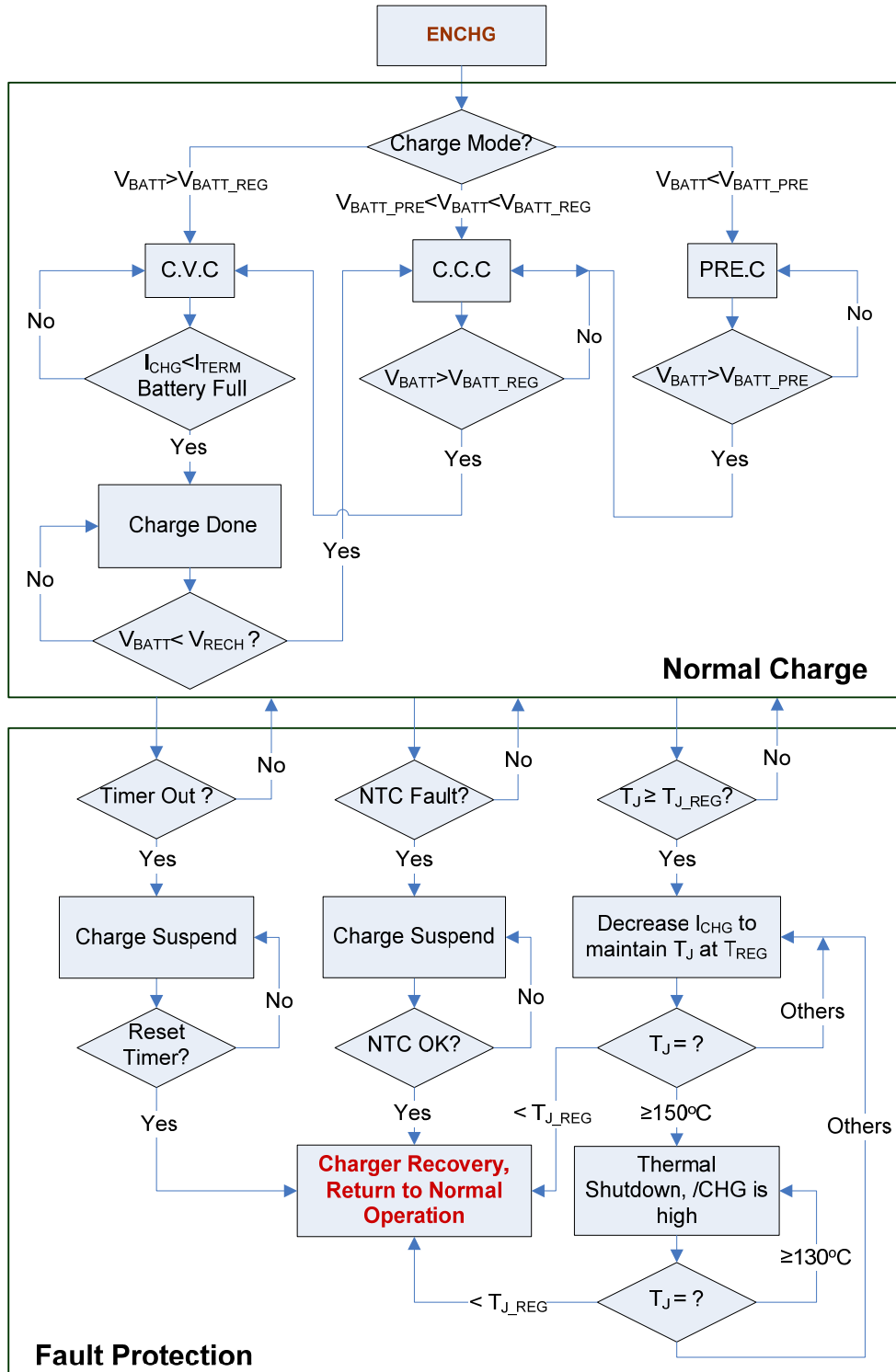


Figure 12: Charging Process



CONTROL FLOW CHART (continued)

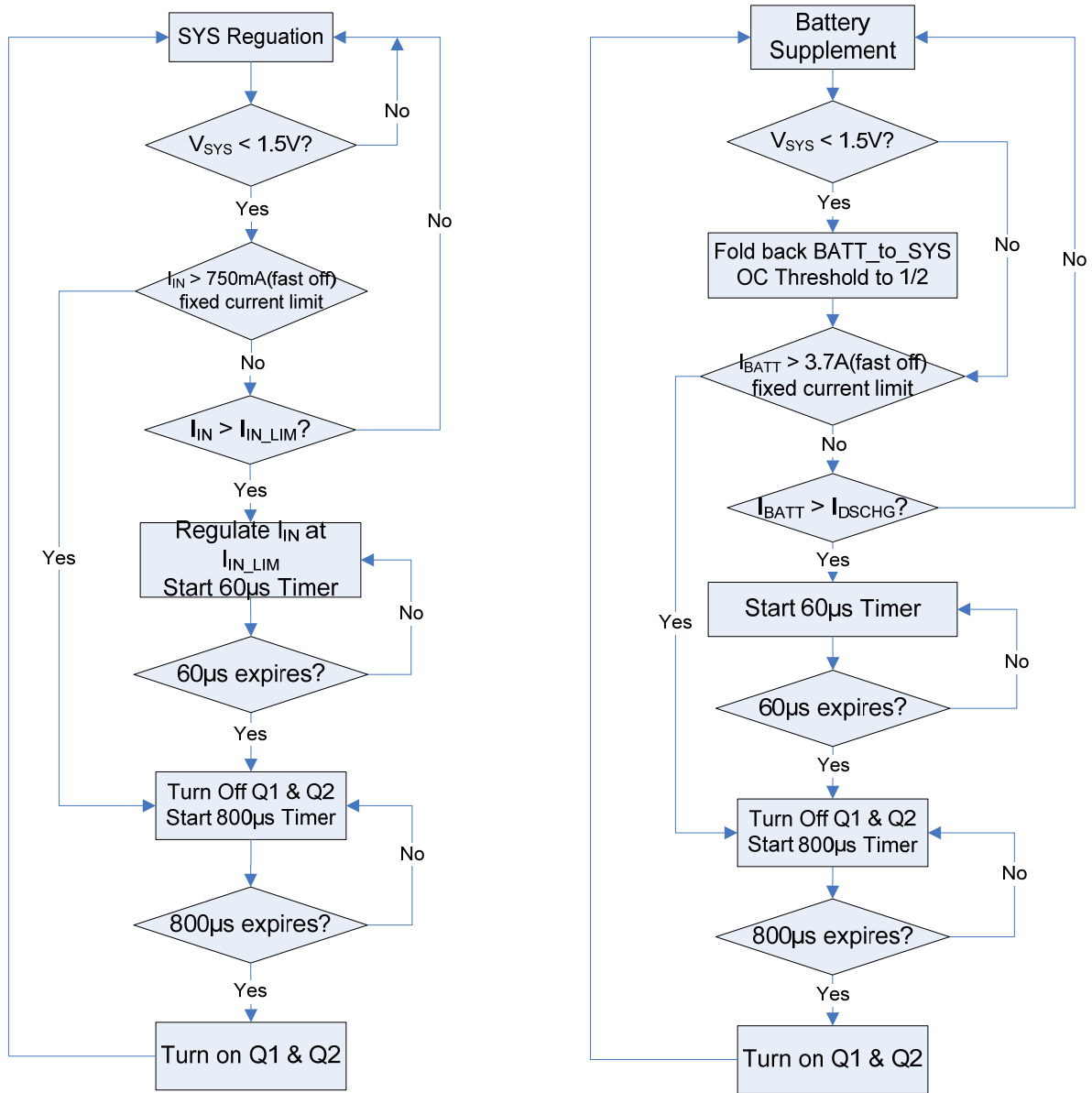
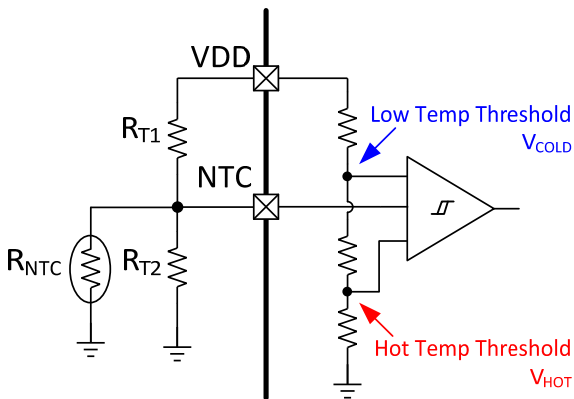


Figure 13: System Short-Circuit Protection

## APPLICATION INFORMATION

### Selecting a Resistor for the NTC Sensor

NTC uses a resistor divider from the input source (VDD) to sense the battery temperature. The two resistors ( $R_{T1}$  and  $R_{T2}$ ) allow the high temperature limit and low temperature limit to be programmed independently (see Figure 14). In other words, the IC can fit most types of NTC resistors and different temperature operation range requirements with the two extra resistors.



**Figure 14: NTC Function Block**

For a given NTC thermistor,  $R_{T1}$  and  $R_{T2}$  depend on the type of NTC resistor used and can be calculated with Equation (1) and Equation (2):

$$R_{T2} = \frac{(V_{COLD} - V_{HOT}) \times R_{NTCH} \times R_{NTCL}}{(V_{HOT} - V_{COLD} V_{HOT}) \times R_{NTCL} - (V_{COLD} - V_{COLD} V_{HOT}) \times R_{NTCH}} \quad (1)$$

$$R_{T1} = \frac{1 - V_{COLD}}{V_{COLD}} \times (R_{T2} // R_{NTCL}) \quad (2)$$

Where  $R_{NTCH}$  is the value of the NTC resistor at the high temperature of the required temperature operating range, and  $R_{NTCL}$  is the value of the NTC resistor at a low temperature.

For example, for thermistor NCP18XH103,  $R_{NTCL}$  is 27.219k $\Omega$  at 0 $^{\circ}$ C, and  $R_{NTCH}$  is 4.161k $\Omega$  at 50 $^{\circ}$ C. Equation (1) and Equation (2) determine that  $R_{T1} = 7.01$ k $\Omega$  and  $R_{T2} = 27.21$ k $\Omega$  (assuming that the NTC window is between 0 $^{\circ}$ C and 50 $^{\circ}$ C and using the  $V_{COLD}$  and  $V_{HOT}$  values from the EC table on page 8).

### Selecting the External Capacitor

Like most low-dropout regulators, the MP2664 requires external capacitors for regulator stability and voltage spike immunity. The MP2664 is designed specifically for portable applications requiring a minimal board space and small components. These capacitors must be selected correctly for optimal performance.

An input capacitor is required for stability. Connect a 1 $\mu$ F (minimum) capacitor between IN and GND for stable operation over the entire load current range. There can be more output capacitance than input as long as the input is at least 1 $\mu$ F.

The IC is designed specifically to work with a very small ceramic output capacitor. A >2.2 $\mu$ F ceramic capacitor with X5R or X7R type dielectrics is suitable in the MP2664 application circuit. For the MP2664, the output capacitor should be connected between SYS and GND with thick traces and a small loop area.

A capacitor from BATT to GND is necessary for the MP2664. A >2.2 $\mu$ F ceramic capacitor with X5R or X7R type dielectrics is suitable for the application circuit.

A capacitor between VDD and GND is used to stabilize the VDD voltage to power the internal control and logic circuit. The typical value of this capacitor is 100nF.

### PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For best results, follow the guidelines below.

1. Place the external capacitors as close to the IC as possible to ensure the smallest input inductance and ground impedance.
2. Place the PCB trace connecting the capacitor between VDD and GND very close to the IC.
3. Keep the GND for the I<sup>2</sup>C wire clean and away from GND.
4. Place the I<sup>2</sup>C wire in parallel.

TYPICAL APPLICATION CIRCUIT

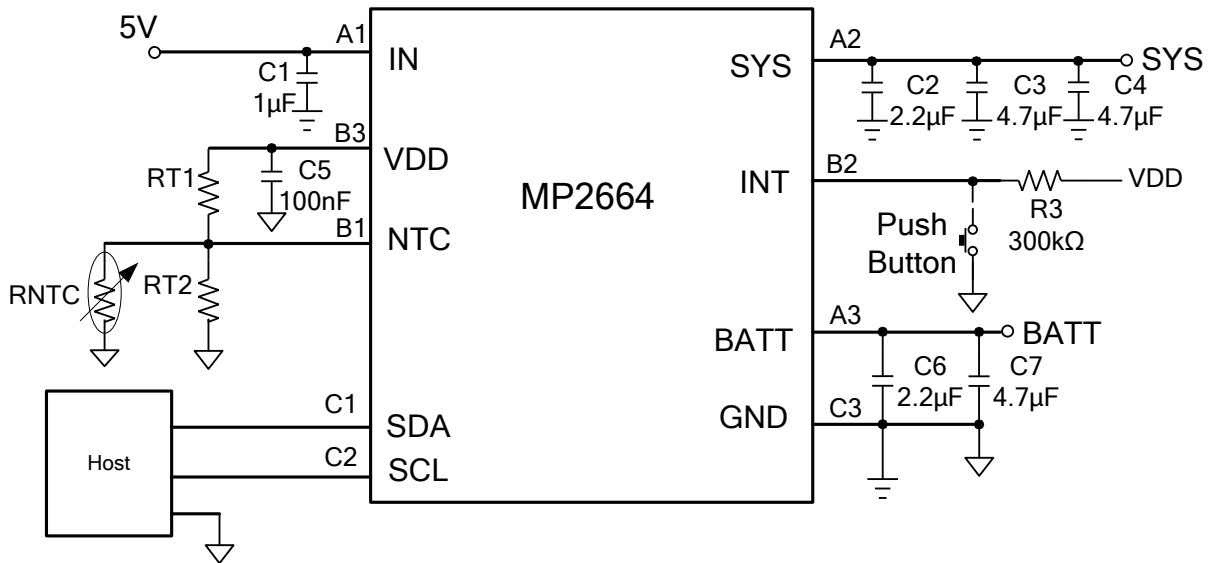


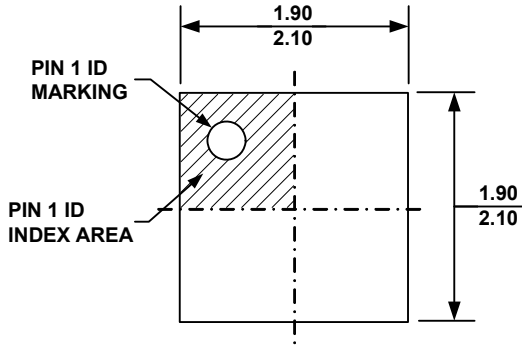
Figure 15: MP2664 Typical Application Circuit with 5V Input

Table 6: Key BOM from Figure 15

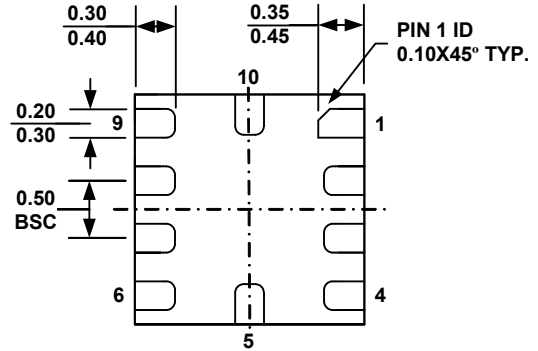
| Qty | Ref        | Value | Description                           | Package | Manufacture |
|-----|------------|-------|---------------------------------------|---------|-------------|
| 1   | C1         | 1µF   | Ceramic Capacitor;16V;<br>X5R or X7R  | 0603    | Any         |
| 2   | C2, C6     | 2.2µF | Ceramic Capacitor;16V;<br>X5R or X7R  | 0603    | Any         |
| 1   | C3, C4, C7 | 4.7µF | Ceramic Capacitor; 16V;<br>X5R or X7R | 0603    | Any         |
| 1   | C5         | 100nF | Ceramic Capacitor;16V;<br>X5R or X7R  | 0603    | Any         |

**PACKAGE INFORMATION**

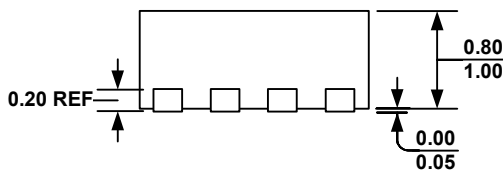
**QFN-10 (2mmx2mm)**



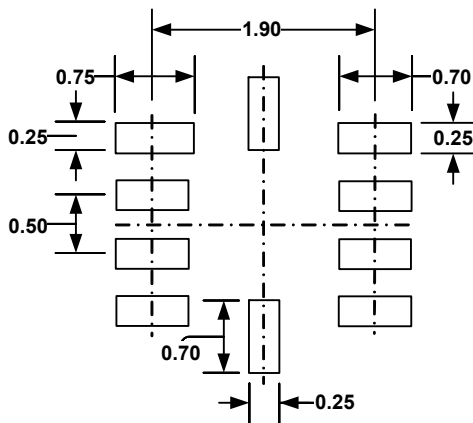
**TOP VIEW**



**BOTTOM VIEW**



**SIDE VIEW**



**RECOMMENDED LAND PATTERN**

**NOTE:**

- 1) ALL DIMENSIONS ARE IN MILLIMETERS.
- 2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
- 3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETER MAX.
- 4) JEDEC REFERENCE IS MO-220, VARIATION VCCD.
- 5) DRAWING IS NOT TO SCALE.

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