

# Hardware Development Guide for the i.MX 7ULP Applications Processor

## 1. Introduction

This document's purpose is to help design and test i.MX 7ULP processor-based designs. It provides information about board layout recommendations, design checklists to ensure first-pass success, and ways to avoid board bring-up problems.

The reader is expected to have a working understanding of board layouts and terminology and common board-hardware terminology.

This guide is released along with relevant device-specific hardware documentation (such as datasheets, reference manuals, and application notes) available on [www.nxp.com](http://www.nxp.com).

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## 1.1. Supported devices

This hardware development guide currently supports the i.MX 7ULP processors.

## 1.2. Essential reference

This guide accompanies the i.MX 7ULP chip reference manuals and data sheets. For the reflow profile and thermal limits during soldering, see *General Soldering Temperature Process Guidelines* (document AN3300). These documents are available on [www.nxp.com](http://www.nxp.com).

## 1.3. Suggested reading

This section lists additional resources that provide background for the information in this guide, as well as general information about the architecture.

### 1.3.1. General information

The following documentation provides useful information about the Arm<sup>®</sup> processor architecture and computer architecture in general.

For Arm Cortex<sup>®</sup>-M4 processor information, see: [www.arm.com/products/processors/cortex-m](http://www.arm.com/products/processors/cortex-m).

For Arm Cortex-A7 processor information, see: [www.arm.com/products/processors/cortex-a](http://www.arm.com/products/processors/cortex-a).

- *Computer Architecture: A Quantitative Approach (Fourth Edition)* by John L. Hennessy and David A. Patterson.
- *Computer Organization and Design: The Hardware/Software Interface (Second Edition)* by David A. Patterson and John L. Hennessy.

The following documentation provides useful information about high-speed board design:

- *Right the First Time- A Practical Handbook on High Speed PCB and System Design - Volumes I & II*—Lee W. Ritchey (Speeding Edge)—ISBN 0-9741936- 0-72.
- *Signal and Power Integrity Simplified (Second Edition)*—Eric Bogatin (Prentice Hall)—ISBN 0-13-703502-0.
- *High Speed Digital Design- A Handbook of Black Magic*—Howard W. Johnson & Martin Graham (Prentice Hall)—ISBN 0-13-395724-1.
- *High Speed Signal Propagation- Advanced Black Magic*—Howard W. Johnson & Martin Graham (Prentice Hall)—ISBN 0-13-084408-X.
- *High Speed Digital System Design - A handbook of Interconnect Theory and Practice*—Hall, Hall and McCall (Wiley Interscience 2000)—ISBN 0-36090-2.
- *Signal Integrity Issues and Printed Circuit Design*—Doug Brooks (Prentice Hall) ISBN 0-13-141884-X.
- *PCB Design for Real-World EMI Control*—Bruce R. Archambeault (Kluwer Academic Publishers Group)—ISBN 1-4020-7130-2.

- *Digital Design for Interference Specifications - A Practical Handbook for EMI Suppression*—David L. Terrell & R. Kenneth Keenan (Newnes Publishing)—ISBN 0-7506-7282-X.
- *Electromagnetic Compatibility Engineering*—Henry Ott (First Edition—John Wiley and Sons)—ISBN 0-471-85068-3.
- *Introduction to Electromagnetic Compatibility*—Clayton R. Paul (John Wiley and Sons)—ISBN 978-0-470-18930-6.
- *Grounding & Shielding Techniques*—Ralph Morrison (Fifth Edition—John Wiley and Sons)—ISBN 0-471-24518-6.
- *EMC for Product Engineers*—Tim Williams (Newnes Publishing)—ISBN 0-7506- 2466-3.

## 1.4. Related documentation

Additional literature is published as new NXP products become available. For a current list of documentation, see [www.nxp.com](http://www.nxp.com).

## 1.5. Conventions

This document uses the following notational conventions:

<i>Courier</i>	Used to indicate commands, command parameters, code examples, and file and directory names.
<i>Italics</i>	<i>Italics</i> indicates command or function parameters.
<b>Bold</b>	Function names are written in bold.
cleared/set	When a bit takes the value of zero, it is said to be cleared. When it takes a value of one, it is said to be set.
<b>mnemonics</b>	Instruction mnemonics are shown in lowercase bold. Book titles in the text are set in italics.
sig_name	Internal signals are written in lowercase.
nnnn nnnnh	Denotes a hexadecimal number.
0b	Denotes a binary number.
rA, rB	Instruction syntax used to identify a source GPR.
rD	Instruction syntax used to identify a destination GPR.
REG[FIELD]	Abbreviations for registers are shown in uppercase. Specific bits, fields, or ranges appear in brackets. For example, MSR[LE] refers to the little-endian mode enable bit in the machine state register.
x	In some contexts (such as signal encodings), an unitalicized x indicates a “don’t care”.
<i>x</i>	An italicized <i>x</i> indicates an alphanumeric variable.
<i>n, m</i>	An italicized <i>n</i> indicates a numeric variable.

### NOTE

In this guide, the notation for all logical, bit-wise, arithmetic, comparison, and assignment operations follows C-language conventions.

## 1.6. Signal conventions

*\_b, \_B* A notation indicates that a signal is active when low.  
*signal\_name* Lowercase italics is used to indicate internal signals.

## 1.7. Acronyms and abbreviations

Table 1 defines the acronyms and abbreviations used in this document.

**Table 1. Definitions and acronyms**

Term	Definitions
Arm	Advanced RISC machines processor architecture
BGA	Ball grid array package
BOM	Bill of materials
BSDL	Boundary scan description language
DDR	Dual data rate DRAM
LPDDR2	Low-power DDR2 SDRAM
LPDDR3	Low-power DDR3 SDRAM
DRAM	Dynamic random access memory
ESR	Equivalent series resistance (of a crystal)
GND	Ground
GPIO	General-purpose input/output
I <sup>2</sup> C	Inter-integrated circuit interface
IBIS	Input-output buffer information specification
IOMUX	Chip-level I/O multiplexing
JTAG	Joint test action group
LDO	Low drop-out regulator
LVDS	Low-voltage differential signaling
MIPI DSI	MIPI display serial interface controller
MMDC	Multi-mode DDR controller
ODT	On-die termination
OTP	One-time programmable
PCB	Printed circuit board
PMIC	Power management integrated circuit
POR	Power-on reset
RAM	Random access memory
ROM	Read-only memory
UART	Universal asynchronous receiver/transmitter
USB	Universal serial bus
USB HSIC	Universal serial bus high-speed inter-chip physical layer
USB OTG	USB on-the-go
USB 2.0	USB version 2.0 peripheral
uSDHC	Ultra-secured digital host controller

## 2. i.MX 7ULP design checklist

The design checklist tables contain recommendations for an optimal design. Where appropriate, the checklist tables also provide an explanation of the recommendation so that you have a greater understanding of why certain techniques are recommended. All supplemental tables referenced by the checklist are in [Section 2.1, “Design checklist tables”](#).

### 2.1. Design checklist tables

**Table 2. DDR recommendations**

Checkbox	Recommendation	Explanation/supplemental recommendation
	Connect ZQPAD to an external 240 $\Omega$ 1% resistor to GND.	This is a reference used during the DRAM output buffer driver calibration.
	Connect DDR_VREF0 and DDR_VREF1 to a source that is 50% of the voltage value of VDD_DDR.	You can tie DDR_VREF to a precision external resistor divider. Shunt the DDR_VREF to GND with a closely-mounted 0.1 $\mu$ F capacitor. See <a href="#">Table 12</a> for resistor values. Using resistors with recommended tolerances ensures the $\pm 2\%$ DDR_VREF tolerance, as per the LPDDR2/LPDDR3 specifications. You can use a PMIC's tracking regulator, as used in NXP reference designs.
	DDR_CKE0 and DDR_CKE1 require external pull-down resistors to GND for the JEDEC compliance when using LPDDR2/LPDDR3.	For LPDDR2/LPDDR3: DDR_CKE[1:0] must be pulled down to meet the JEDEC sequence until the controller is configured and starts driving. NXP designs use 10 k $\Omega$ .
	DDR_CKE0 and DDR_CKE1 require external resistors (such as 10 k $\Omega$ ) to GND to minimize current drain during the deep-sleep mode (DSM).	During low-power self-refresh, the BSP programs the pad control register GRP_CTLDS to 0x00000000. Therefore, DDR_CKE0, DDR_CKE1, and other associated GRP_CTLDS I/O are forced to the high-impedance state. Because DDR_CKE0 and DDR_CKE1 are forced to high-Z, external pull-down resistors are required to avoid floating outputs during standby. In NXP designs, 10-k $\Omega$ resistors are used for this purpose. Any other termination on the DDR_CKE0 and DDR_CKE1 lines (such as 50 $\Omega$ ) must not be present; a simulation must be performed to ensure CKE signal integrity.

**Table 3. Boot mode input recommendations**

Checkbox	Recommendation	Explanation/supplemental recommendation
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	<p>For BOOT_MODE1 and BOOT_MODE0, use one of these options to achieve logic 0:</p> <ul style="list-style-type: none"> <li>• Tie to GND through an external resistor of any size.</li> <li>• Tie directly to GND.</li> <li>• Leave unconnected.</li> </ul> <p>Use one of these options to achieve logic 1:</p> <ul style="list-style-type: none"> <li>• Tie directly to VDD_PTB.</li> <li>• Tie to VDD_PTB through an external 10 kΩ resistor. A value of 4.7 kΩ is preferred in high-noise environments.</li> </ul> <p>If switch control is desired, no external pull-down resistors are necessary. Simply connect the SPST switches directly to the VDD_PTB rail. If desired, a 4.7 kΩ to 10 kΩ series resistor can be used when the current drain is critical.</p>	<p>Boot inputs BOOT_MODE1 and BOOT_MODE0 each have on-chip pull-down devices. Be aware that when these are logic-high, current is drawn from the VDD_PTB supply. In production, when the on-chip fuses determine the boot configuration, both boot mode inputs can remain unconnected.</p>
	<p>The BT0_CFGn and BT1_CFGn signals are required for a proper functionality and operation and must not remain unconnected when the chip boot configuration is not determined by the fuses (during development).</p>	<p>See the “System Boot” chapter in the chip reference manual for the correct boot configuration. Note that an incorrect setting may result from an improper booting sequence. In production, when the on-chip fuses determine the boot configuration, both boot mode inputs can remain unconnected.</p>

**Table 4. I<sup>2</sup>C recommendations**

Checkbox	Recommendation	Explanation/supplemental recommendation
	Verify the target I <sup>2</sup> C interface clock rates.	The bus can only operate as fast as the slowest peripheral on the bus. If faster operation is required, move the slow devices to another I <sup>2</sup> C port.
	Verify that the target I <sup>2</sup> C address range is supported and does not conflict with other peripherals. If there is an unavoidable address conflict, move the offending device to another I <sup>2</sup> C port.	If it is undesirable to move the conflicting device to another I <sup>2</sup> C port, review the peripheral operation to see if it supports address remapping.
	Do not place more than one set of pull-up resistors on the I <sup>2</sup> C lines.	This can result in excessive loading. A good design practice is to place one pair of pull-ups only.

**Table 5. JTAG recommendations**

Checkbox	Recommendation	Explanation/supplemental recommendation
	Ensure that the on-chip pull-up/pull-down configuration is followed when external resistors are used with the JTAG signals. For example, do not use an external pull-down on an input that has an on-chip pull-up.	External resistors can be used with all JTAG signals, but they are not required. See <a href="#">Table 13</a> for a summary of the JTAG interface.

**Table 6. Power and decoupling recommendations**

Checkbox	Recommendation	Explanation/supplemental recommendation
	Comply with the power-up sequence guidelines, as described in the data sheet to guarantee	Any deviation from these sequences may result in these situations:

Checkbox	Recommendation	Explanation/supplemental recommendation
	reliable operation of the device.	<ul style="list-style-type: none"> <li>Excessive current during the power-up phase.</li> <li>Prevention of the device from booting.</li> <li>Irreversible damage to the processor.</li> </ul>
	Maximum ripple voltage requirements.	A common requirement for the ripple noise must be less than 5% Vp-p of the supply voltage average value.
	The CM4 domain LDO supply is always operated in the LDO-enabled mode. The LDO-bypassed mode is not supported for this LDO. VDD_PMC11_DIG0_CAP must be connected to VDD_DIG0 at the board level. The maximum DC impedance for this connection is 50 mΩ.	—
	The CA7 domain LDO supply can be operated in the LDO-enabled mode. If so, VDD_PMC11_DIG1_CAP must be connected to VDD_DIG0 at the board level. The maximum DC impedance for this connection is 50 mΩ.	—

Table 7. Power supply decoupling recommendations

Checkbox	Supply	0.22 μF	1 μF	2.2 μF	4.7 μF	10 μF	22 μF
	VDD_VBAT42	1				1	
	VDD_VBAT18_CAP	1		1			
	VDD_PMC18	1					
	VDD18_IOREF	1					
	VDD_PMC18_DIG0	2					1
	VDD_PMC11_DIG0_CAP	1				1	
	VDD_DIG0	2					
	VDD_PMC12_DIG1	1			1		
	VDD_PMC11_DIG1_CAP	1		1			
	VDD_DIG1	9			1		1
	VDD_PTA	2			1		
	VDD_PTB	2					
	VDD_PTC	2					
	VDD_PTD	2			1		
	VDD_PTE	2			1		
	VDD_PTF	2					
	VDD_HSIC	1					
	VDD_DDR		4				1
	VDD18_DDR	2					1
	VDD_DSI11	1					
	VDD_DSI18	1					
	VDD_USB18	1					
	VDD_USB33	1					
	VDD_PLL18	1					
	VREFH_ANA18	1					
	VDD_ANA18	1					
	VDD_ANA33	1					

**NOTE**

Use the smallest capacitor package size allowed by your design rules.

For the 0.22- $\mu$ F capacitors, use the 0201 or 0402 package sizes (0201 is recommended).

For the 2.2- $\mu$ F capacitors, the 0402 package is recommended.

For the 22- $\mu$ F capacitors, the 0603 package is recommended.

On VDD\_DDR, four 1- $\mu$ F capacitors were used on the i.MX 7ULP EVK, based on the power distribution network analysis of that design. Four 0.22- $\mu$ F capacitors are also acceptable.

**Table 8. Oscillator and clock recommendations**

Checkbox	Recommendation	Explanation/supplemental recommendation
	Precision 32.768-kHz oscillator: <ul style="list-style-type: none"> <li>• Connect a crystal between EXTAL32 and XTAL32.</li> <li>• Choose a crystal with a maximum ESR (equivalent series resistance) of 70 k<math>\Omega</math> and a drive level of at least 0.5 <math>\mu</math>W.</li> <li>• Follow the manufacturer's recommendation for loading capacitance.</li> <li>• Do not use an external biasing resistor because the bias circuit is on the chip.</li> </ul>	The capacitors implemented on either side of the crystal are about twice the crystal load capacitance. To achieve the target oscillation frequency, board capacitors must be reduced to compensate for board and chip parasitic capacitance; typically, 15–16 pF is employed. The integrated oscillation amplifier has an on-chip self-biasing scheme but is high-impedance (relatively weak) to minimize power consumption. Care must be taken to limit parasitic leakage from EXTAL32 and XTAL32 to either the power or the ground (> 100 M $\Omega$ ) because this negatively affects the amplifier bias and causes a reduction of the startup margin. Use short traces between the crystal and the processor, with a ground plane under the crystal, load capacitors, and associated traces.
	External kilohertz source: <ul style="list-style-type: none"> <li>• If feeding an external clock into the device, EXTAL32 can be driven DC-coupled with the XTAL32 left unconnected or driven with a complimentary signal.</li> </ul>	The voltage level of this driving clock must not exceed the voltage of VDD_VBAT18_CAP and the frequency must be <100 kHz under typical conditions. Do not exceed VDD_VBAT18_CAP or damage/malfunction may occur. The EXTAL32 signal must not be driven if the VDD_VBAT18_CAP supply is off. This can lead to damage or malfunction. Note that if this external clock is stopped, the internal ring oscillator starts automatically.
	Precision 24-MHz oscillator: <ul style="list-style-type: none"> <li>• Connect a fundamental-mode crystal between EXTAL0 and XTAL0.</li> <li>• Choose a crystal with a maximum ESR (equivalent series resistance) of 100 <math>\Omega</math> and drive level of at least 150 <math>\mu</math>W.</li> <li>• Do not use an external biasing resistor because the bias circuit is on the chip.</li> </ul>	The NXP BSP software requires 24 MHz on this clock. This clock is used as a reference for the USB, so there are strict frequency tolerance and jitter requirements. See <a href="#">Table 14</a> for guidelines. To access a calculator for the 24-MHz crystal drive level, see the engineering bulletin EB830 on the i.MX community.
	Use an external megahertz source if feeding an external clock into the device. EXTAL0 can be driven DC-coupled with the XTAL0 floating.	The NXP BSP software requires 24 MHz on this clock. This clock is used as a reference for the USB, so there are strict frequency tolerance and jitter requirements. See <a href="#">Table 14</a> for guidelines.



**Table 9. Reset and ON/OFF recommendations**

Checkbox	Recommendation	Explanation/supplemental recommendation
	RESET0_b must be asserted immediately at power-up and remain asserted until the real-time domain power supplies are powered and stable. See the "Power-on sequencing" section of the i.MX 7ULP data sheet for a list of real-time domain power supplies.	—
	For portable applications, the ON/OFF (button) input may be connected to the ON/OFF SPST push-button. On-chip debouncing is provided, and this input has an on-chip pull-up. If not used, ON/OFF must remain unconnected.	A brief connection to GND in the OFF mode causes the internal power management state machine to change the state to ON. In the ON mode, a brief connection to GND generates an interrupt (intended to be a software-controllable power-down). A 5-second (or longer) connection to the GND causes a forced OFF.
	RESET0_b and RESET1_b must not be tied together at the board level.	RESET0_b is the power-on reset signal for the CM4 domain (real-time domain). When the CM4 core is in reset, RESET0_b is driven low as an open-drain output. When the CM4 core is not in reset, RESET0_b is an input with an on-chip pull-up. At the system level, the system must reset the i.MX 7ULP (POR) by pulling RESET0_b low. RESET1_b is the reset indication associated with the CA7 core. When the CA7 core is in reset, RESET1_b is driven low as an open-drain output. When the CA7 core is not in reset, RESET1_b is an input with an on-chip pull-up. RESET1_b must not be used as an input to reset the CA7 core from outside the chip. This is not a valid use case and results in unpredictable behavior. The CA7 core must always be reset by the CM4 core internally. RESET1_b must remain unconnected unless it is used as an indication to the system that the CA7 core has entered reset. RESET0_b and RESET1_b must not be tied together at the board level.

**Table 10. USB recommendations**

Checkbox	Recommendation	Explanation/supplemental recommendation
	USB OTG: <ul style="list-style-type: none"> <li>To comply with the USB OTG specification, the VBUS supply on the OTG connector must default to <i>off</i> when the boards power up.</li> </ul>	The processor must turn the VBUS <i>on</i> as required.

**Table 11. Miscellaneous recommendations**

Checkbox	Recommendation	Explanation/supplemental recommendation
	For termination of unused analog interfaces, see the data sheet for this part.	—
	NC contacts must remain unconnected.	Depending on the feature set, some versions of the IC may have NC contacts connected inside the BGA.
	If MIPI DSI is used, VDD_DSI11 must be connected to VDD_DIG1 at the board level.	—
	VDD_PMC18 and VDD_PTB must be powered from the same source.	These two supplies are connected inside the processor.
	VDD_ANA33 and VDD_PTA must be powered from the same source.	A 120-Ω ferrite bead is recommended to provide AC isolation between the digital supply (VDD_PTA) and the analog supply (VDD_ANA33).
	AC isolation must be provided between VDD_ANA18 and the digital 1.8-V supply it is connected to.	A 120-Ω ferrite bead is recommended to provide AC isolation between the analog supply (VDD_ANA18) and the digital 1.8-V supply it is connected to (VDD_PTB or VDD_PMC18_DIG0).

## 2.2. DDR reference circuit

Table 12 is a resistor chart that provides the recommended DDR\_VREF resistor divider values. The recommendations are appropriate for designs with DDR memory chips with a maximum Vref input current of 2 μA each. The i.MX 7ULP DDR\_VREF0/1 input leakage current is 1 μA for both inputs combined.

**Table 12. Recommended DDR\_VREF resistor divider values**

Number or DRAM with 2 μA Vref input current	Resistor divider value (two resistors)
1	≤ 2.0 kΩ 1%
1	< 5.0 kΩ 0.5%
1	< 7.4 kΩ 0.1%
2	≤ 1.2 kΩ 1%
2	< 3.0 kΩ 0.5%
2	< 4.4 kΩ 0.1%

## 2.3. JTAG signal termination

Table 13 provides the JTAG interface termination requirements.

**Table 13. JTAG interface termination requirements**

JTAG signal	I/O type	On-chip termination	External termination
JTAG_TCK	Input	Programmable (default Hi-z)	Not required: can use 10-kΩ pull-up
JTAG_TMS	Input	Programmable (default Hi-z)	Not required: can use 10-kΩ pull-up
JTAG_TDI	Input	Programmable (default Hi-z)	Not required: can use 10-kΩ pull-up
JTAG_TDO	3-state output	Programmable (default Hi-z)	100-kΩ pull-up recommended
JTAG_TRST_b	Input	Programmable (default Hi-z)	Not required: can use 10-kΩ pull-up

## 2.4. Oscillator tolerance

Table 14 provides the 24-MHz oscillator tolerance guidelines. The designer must verify all tolerances per the official specifications.

**Table 14. 24-MHz crystal tolerance guidelines**

Interface	Tolerance ( $\pm$ ppm)
USB 2.0	500

## 2.5. Unused analog interfaces

For recommendations for unused interfaces, see the “Requirements for unused interfaces” section in the i.MX 7ULP data sheet.

# 3. i.MX 7ULP layout recommendations

## 3.1. Introduction

This chapter provides recommendations to help you with the layout of your i.MX 7ULP-based system.

## 3.2. Basic design recommendations

The i.MX 7ULP processor comes in multiple packages. For detailed information, see the i.MX 7ULP data sheet and reference manual.

When using the Allegro tool, the optimal practice is to use the footprint created by NXP. When not using the Allegro tool, use the Allegro footprint export feature (supported by many tools). If export is not possible, create the footprint per the package mechanical dimensions outlined in the product data sheet.

Native Allegro layout and Gerber files are available on the NXP website upon product release. Contact your local sales office or field applications engineer to check the availability of information before product releases.

### 3.2.1. Placement of decoupling capacitors

Place small decoupling and larger bulk capacitors on the bottom side of the PCB.

The 0201 decoupling and 0603 bulk capacitors must be mounted as close to the power vias as possible. The distance must be less than 50 mils. Additional bulk capacitors can be placed near the edge of the BGA via array. Placing the decoupling capacitors close to the power balls is critical to minimize inductance and ensure high-speed transient current demand by the processor.

A correct via size is critical to preserve adequate routing space. The recommended geometry for the via pads is: pad size of 18 mils and drill of 8 mils.

The following list provides the main recommendations for choosing the correct decoupling scheme:

- Place the largest capacitance in the smallest package that the budget and manufacturing can support.
- For high-speed bypassing, select the required capacitance with the smallest package (for example, 0.22  $\mu$ F and package 0201).
- Minimize the trace length (inductance) to small caps.

- Series inductance cancels out capacitance.
- Tie the capacitors to the GND plane directly with a via.
- Place the capacitors close to the power contact of the associated package designed from the schematic.

An example of good design practices for the BGA power decoupling design is the layout of the i.MX 7ULP EVK available on the NXP website upon product release. Contact your local sales office or field applications engineer to check the availability of information before product releases.

### 3.3. Stack-up recommendations

A high-speed design requires a good stack-up to have the right impedance for the critical traces. The constraints for the trace width may depend on several factors, such as the board stack-up and associated dielectric and copper thickness, required impedance, and required current (for power traces). The NXP reference design uses a minimum trace width of 3 mils for the DDR routing. The stack-up also determines the constraints for routing and spacing.

Consider the following when designing a stack-up and selecting material for your board:

- Board stack-up is critical for high-speed signal quality.
- Preplan the impedance of critical traces.
- High-speed signals must have reference planes on adjacent layers to minimize cross-talk.
- NXP i.MX 7ULP EVK equals Isola IT-180A.

The recommended stack-up for the 14 mm x 14 mm VP package is four to six layers. i.MX 7ULP EVK uses four layers. The stack-up information for i.MX 7ULP EVK is shown in [Table 15](#) and [Table 16](#).

**Table 15. i.MX 7ULP EVK PCB stack-up information**

Layer	Layer type	Finished copper weight
1	Top (component) side	1/2 oz
2	Ground plane	1 oz
3	Power plane	1 oz
4	Bottom side	1/2 oz

**Table 16. i.MX 7ULP EVK PCB stack-up implementation**

Layers	Single-ended		Differential					
	Trace width (mils)	Impedance ( $\Omega$ )	Trace width (mils)	Trace spacing 'airgap' (mils)	Impedance ( $\Omega$ )	Trace width (mils)	Trace spacing 'airgap' (mils)	Impedance ( $\Omega$ )
TOP	4	50	4.5	4	90	3.9	5	100
BOTTOM	4	50	4.5	4	90	3.9	5	100

The recommended stack-up for the 10 mm x 10 mm VK package is eight layers (two ground planes, two power planes, and four signal layers).

### 3.4. DDR connection information

Figure 1 shows the block diagram of the LPDDR2/LPDDR3 interface of i.MX 7ULP EVK.

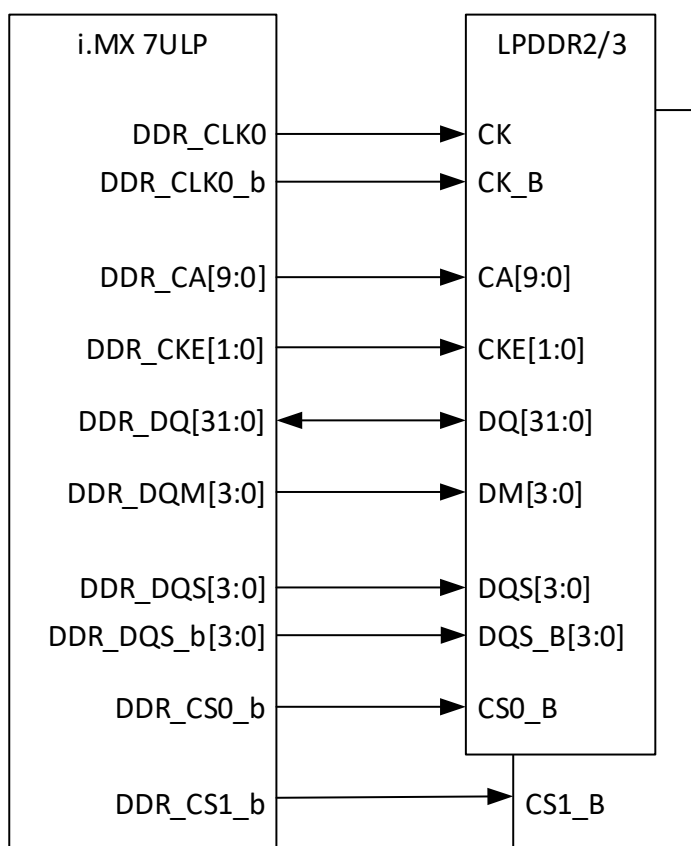


Figure 1. LPDDR2/LPDDR3 interface connections

#### 3.4.1. DDR routing rules

The LPDDR2/3 routing can be accomplished in two different ways: routing all signals at the same length or routing them by the byte group.

Routing all signals at the same length can be more difficult because of the tight space between the DDR and the processor and the large number of required interconnections. However, it is the better way because it makes the signal-timing analysis straightforward. Ideally, all the signals should be routed at the same length. Table 17 explains the rules for routing the signals by the same length.

**Table 17. DDR routing by the same length**

Signals	Total length	Recommendations
Address and bank	Clock length	Match the signals $\pm 25$ mils of the value specified in the length column.
Data and buffer	Clock length	Match the signals $\pm 25$ mils of the value specified in the length column.
Control signals	Clock length	Match the signals $\pm 25$ mils of the value specified in the length column.
Clock DDR_CLK0 and DDR_CLK0_b	Longest trace $\leq 3$ inches	Match the signals for the differential clock pair within $\pm 5$ mils.
DDR_DQS[3:0] and DDR_DQS_b[3:0]	Clock length	Match the DQS signals $\pm 10$ mils of the value specified in the length column.

Routing by a byte group requires a better control of the signals in each group. It is also more difficult for the analysis and constraint settings. However, its advantage is that the constraint to match the lengths can be applied to a smaller group of signals. This is often more achievable when the constraints are properly set. [Table 18](#) explains the rules for routing the signals by byte groups.

**Table 18. LPDDR2/LPDDR3 routing by byte groups**

Chip signals	Group	Length (mils)		Recommendations
		Min	Max	
DDR_CLK0 DDR_CLK0_b	Clock	As short as possible	2.25 inches	Match the signals $\pm 5$ mils. 2.25 inches is recommended.
DDR_CA[9:0] DDR_RAS DDR_CAS DDR_SDWE	Address and command	Clock (min) – 200	Clock (min) <sup>1</sup>	Match the signals $\pm 25$ mils.
DDR_D[7:0] DDR_DQM0 DDR_SDQS0 DDR_SDQS0_b	Byte group 1	—	Clock (min)	Match the signals of each byte group $\pm 25$ mils. Match the differential signals of the DQS $\pm 10$ mils.
DDR_D[15:8] DDR_DQM1 DDR_SDQS1 DDR_SDQS1_b	Byte group 2	—	Clock (min)	
DDR_D[23:16] DDR_DQM2 DDR_SDQS2 DDR_SDQS2_b	Byte group 3	—	Clock (min)	
DDR_D[31:24] DDR_DQM3 DDR_SDQS3 DDR_SDQS3_b	Byte group 4	—	Clock (min)	
DDR_CA[9:0] DDR_CKE[1:0] DDR_CS0_b DDR_CS1_b	Control signals	Clock (min) – 200	Clock (min)	Match the signals $\pm 50$ mils.

1. Clock (min) — The shortest length of the clock group signals because this group has a  $\pm 5$  mil matching tolerance.

### 3.5. High-speed routing recommendations

The following list provides the recommendations for routing the traces of high-speed signals. Note that the propagation delay and the impedance control must match to achieve correct communication with the devices.

- High-speed signals must not cross gaps in the reference plane.
- Avoid creating slots, voids, and splits in the reference planes. Review the via voids to ensure they do not create splits (space out vias).
- Provide the ground return vias within a 100 mil distance from the signal layer-transition vias when transitioning between different reference ground planes.
- A solid ground plane must be directly under the crystal, associated components, and traces.
- Separate the parallel running traces by not less than 2x the dielectric width to the referenced ground plane.
- The clocks or strobes that are on the same layer need at least 2.5x the spacing from an adjacent trace (2.5x the height from a reference plane) to reduce cross-talk.
- All synchronous modules must have bus-length matching and relative clock-length control.
- If space is available, consider routing the pairs of high-speed signals together with a ground trace in between. The ground trace serves as a direct ground-return path. This technique is known as routing “triplets”.

For SD/eMMC interfaces:

- Match the data and the CMD trace lengths (the length delta depends on the bus rates).
- CLK must be longer than the longest signal in the data/CMD group (+5 mils).
- Similar DDR rules must be followed for data, address, and control, as for the SD module interfaces.

The following signals on the i.MX 7ULP are considered high-speed signals and must be routed according to the requirements stated in this document:

- MMDC signals (LPDDR2/LPDDR3 interface).
- USB OTG signals:
  - USB0\_DP/USB0\_DP (differential pair).
- USB HSIC signals:
  - HSIC\_DATA.
  - HSIC\_STROBE.
- MIPI DSI signals (MIPI display serial interface):
  - DSI\_CLK\_P/DSI\_CLK\_N (differential pair).
  - DSI\_DATA0\_P/DSI\_DATA0\_N (differential pair).
  - DSI\_DATA1\_P/DSI\_DATA1\_N (differential pair).
- uSDHC signals (SD/eMMC interfaces).

### 3.5.1. Ground plane recommendations

This section provides examples of good practices and how to avoid common mistakes when flowing the ground planes' layers. [Figure 2](#) and [Figure 3](#) show examples of common poor GND planes.

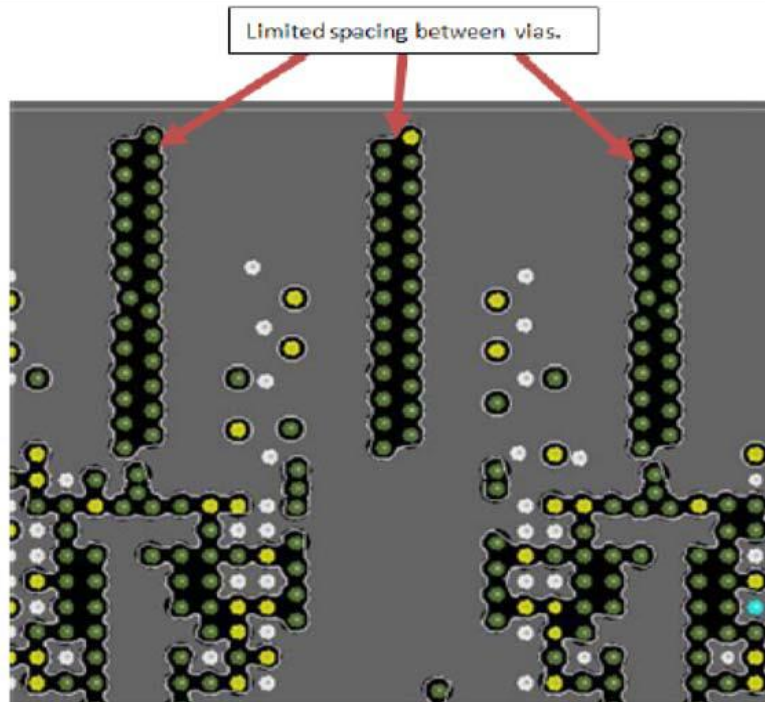


Figure 2. Poor GND plane 1

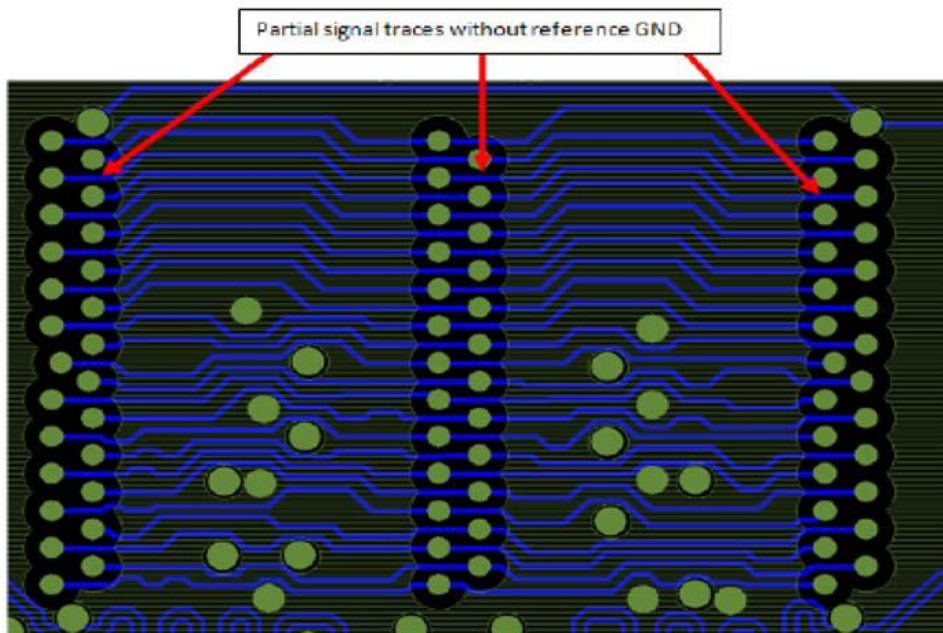


Figure 3. Poor GND plane 2



Spacing the vias some mils apart facilitates the GND copper flowing in the plane. [Figure 4](#) and [Figure 5](#) show good practices of GND planes.

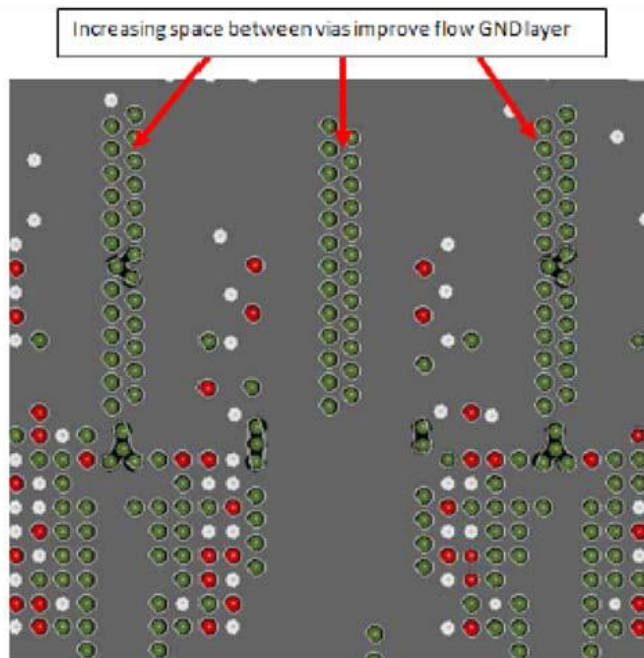


Figure 4. Good layout GND plane detail

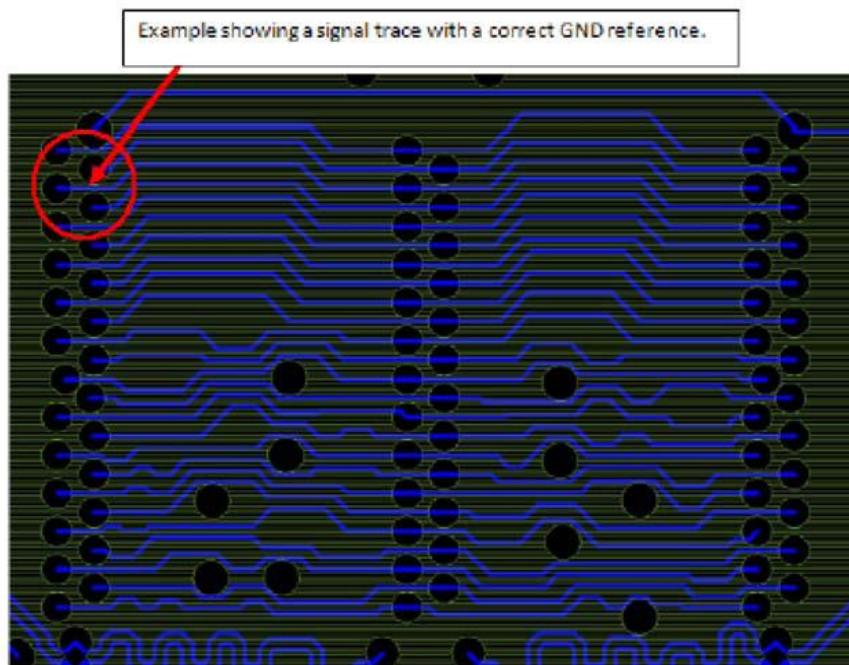


Figure 5. Good layout GND plane detail

### 3.6. DDR power recommendations

These recommendations apply to the DDR\_VREF voltage reference plane:

- Use a 30 mil trace between the decoupling cap and the destination.
- Maintain a 25 mil clearance from other nets.
- Isolate the VREF and/or shield with GND.

Decouple using distributed 0.22  $\mu\text{F}$  capacitors by the regulator, controller, and devices.

- Place 1.0  $\mu\text{F}$  capacitors near the VREF source. One near the VREF pin on the controller and two between the controller and the devices.

### 3.7. USB recommendations

Follow these recommendations for the USB:

- Route the high-speed clocks and the DP and DM differential pair first.
- Route the DP and DM signals on the top or bottom layer of the board.
- The trace width and spacing of the DP and DM signals must meet the differential impedance requirement of 90  $\Omega$ .
- Route the traces over the continuous planes (power and ground).
  - Traces must not pass over any power/ground-plane slots or anti-etch.
  - When placing the connectors, make sure that the GND plane clear-outs around each pin have ground continuity between all pins.
- Maintain the parallelism (skew matching) between DP and DM, and match the overall differential length difference to less than 5 mils.
- Maintain symmetric routing for each differential pair.
- Do not route the DP and DM traces under the oscillators or parallel to the clock traces and/or data buses.
- Minimize the lengths of high-speed signals that run in parallel to the DP and DM pair.
- Keep the DP and DM traces as short as possible.
- Route the DP and DM signals with a minimum number of corners. Use 45-degree turns instead of 90-degree turns.
- Avoid layer changes (vias) on the DP and DM signals. Do not create stubs or branches.
- Provide the ground return vias within a 50 mil distance from the signal layer-transition vias when transitioning between different reference ground planes.

### 3.8. Impedance signal recommendations

Use [Table 19](#) as a reference when updating or creating constraints in your software PCB tool to set up the impedance and the correct trace width.

**Table 19. Impedance signal recommendations**

Signal group	Impedance	Layout tolerance
All signals, unless specified	50 $\Omega$ single-ended	$\pm 10\%$

Signal group	Impedance	Layout tolerance
Differential signals: USB and MIPI DSI	90 $\Omega$ differential	$\pm 10\%$
Differential signals: DDR	100 $\Omega$ differential	$\pm 10\%$

Figure 6 shows the dimensions of a stripline and a microstrip pair. Figure 7 shows the differential pair routing.

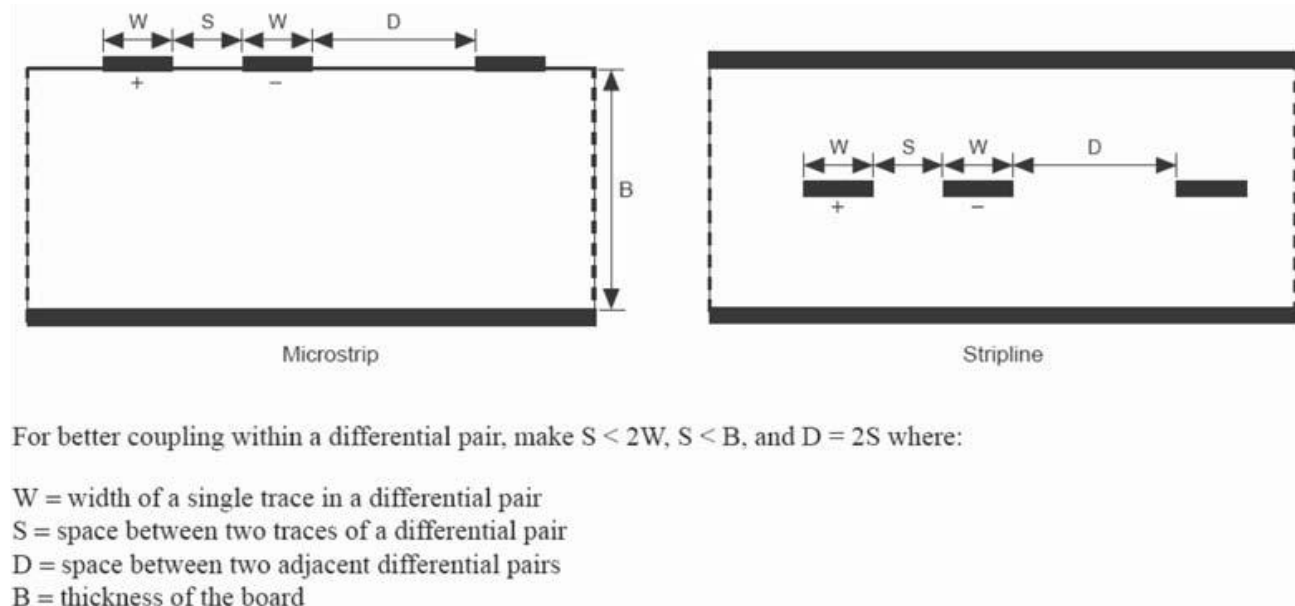


Figure 6. Microstrip and stripline differential pair dimensions

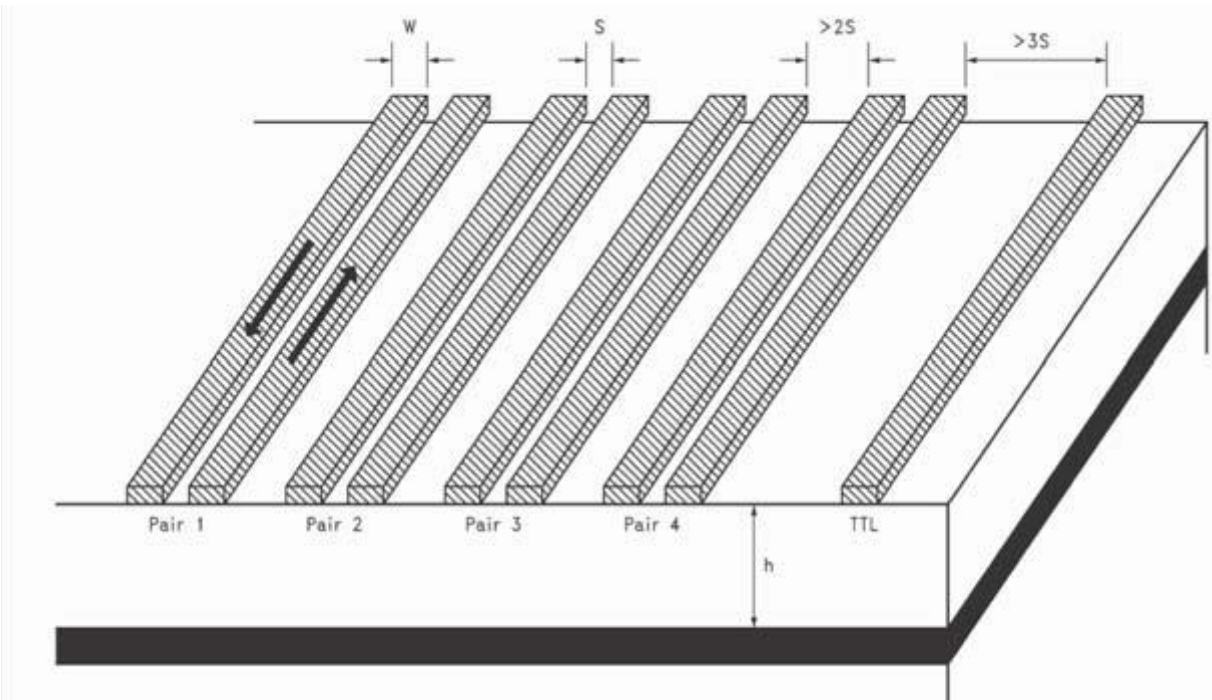


Figure 7. Differential pair routing

- The space between two adjacent differential pairs must be greater than or equal to twice the

space between the two individual conductors.

- The skew between the LVDS pairs must be within the minimum recommendation ( $\pm 100$  mils).

### 3.9. Reference resistors

#### NOTE

The reference resistor and the connection must be placed away from noisy regions. The noise induced on it may impact the internal circuit and degrade the interface signals.

### 3.10. ESD and radiated emissions recommendations

The PCB design must use solid power and ground planes. The recommendations for ESD immunity and radiated emissions performance are as follows:

- All components with ground chassis shields (USB jack, buttons, and so on) must connect the shield to the PCB chassis ground ring.
- Ferrite beads must be placed on each signal line connected to an external cable. These ferrite beads must be placed as close to the PCB jack as possible.

#### NOTE

Ferrite beads must have a minimum impedance of  $500 \Omega$  at 100 MHz (except for the ferrite on USB0 VBUS).

- Ferrite beads must not be placed on the USB DP/DM signal lines, because this can cause USB signal integrity problems. For radiated emissions problems due to USB, a common-mode choke can be placed on the DP/DM signal lines. However, it should not be required if the PCB layout is satisfactory. Ideally, the common-mode choke must be approved for high-speed USB use or tested thoroughly to verify that there are no signal integrity issues.
- It is highly recommended to use ESD protection devices on the ports connected to external connectors. See the reference schematic (available at [www.nxp.com](http://www.nxp.com)) for detailed information about the ESD protection implementation on USB interfaces.
- If possible, stitch all around the board with vias with a 100-mil spacing between them, and connect the vias to the GND planes with exposed solder mask to improve EMI.

### 3.11. Component placement recommendations

Adhere to these recommendations when placing components:

- Place the components in such way that short and/or critical routes can be easily laid out:
  - Critical routes determine the component location.
  - Position the devices to facilitate routes (minimize the length and crossovers).
- Consider placing these pairings adjacent:
  - i.MX and DDR.
  - PHY and associated jack.

- Jack and CODEC input.
- Bluetooth® (or other RF) and antenna.

### 3.12. Reducing skew and phase problems in differential pairs' traces

The differential pair technology has evolved to require more stringent checking around phase control. This is evident from the higher data rates associated with parallel buses (such as DDR and LVDS). Simply put, the differential pair technology sends opposite and equal signals down a pair of traces. Keeping these opposite signals in phase is essential to ensure that they work as intended.

Figure 8 and Figure 9 show two examples of static routing where a match is achieved without the need to tune one element of the differential pair.

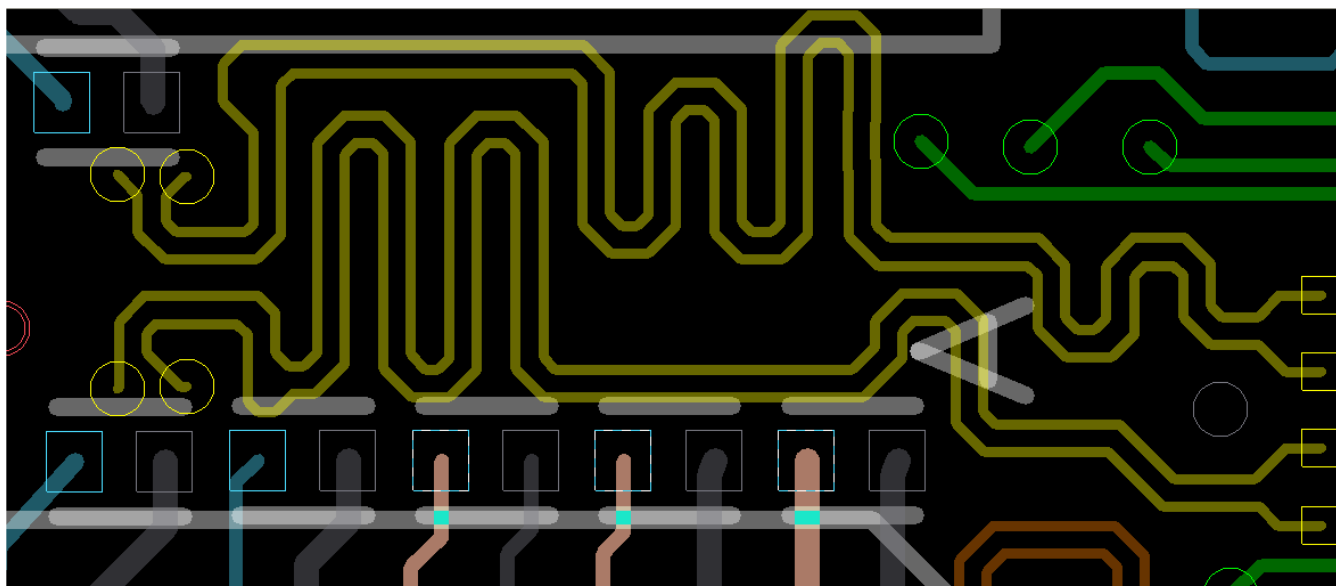


Figure 8. Yellow traces differential pairs 1

Figure 9 shows the addition of a delay trace to one element of the differential pair to avoid length mismatch (which reduces skew and phase problems). The green box marks the detail.

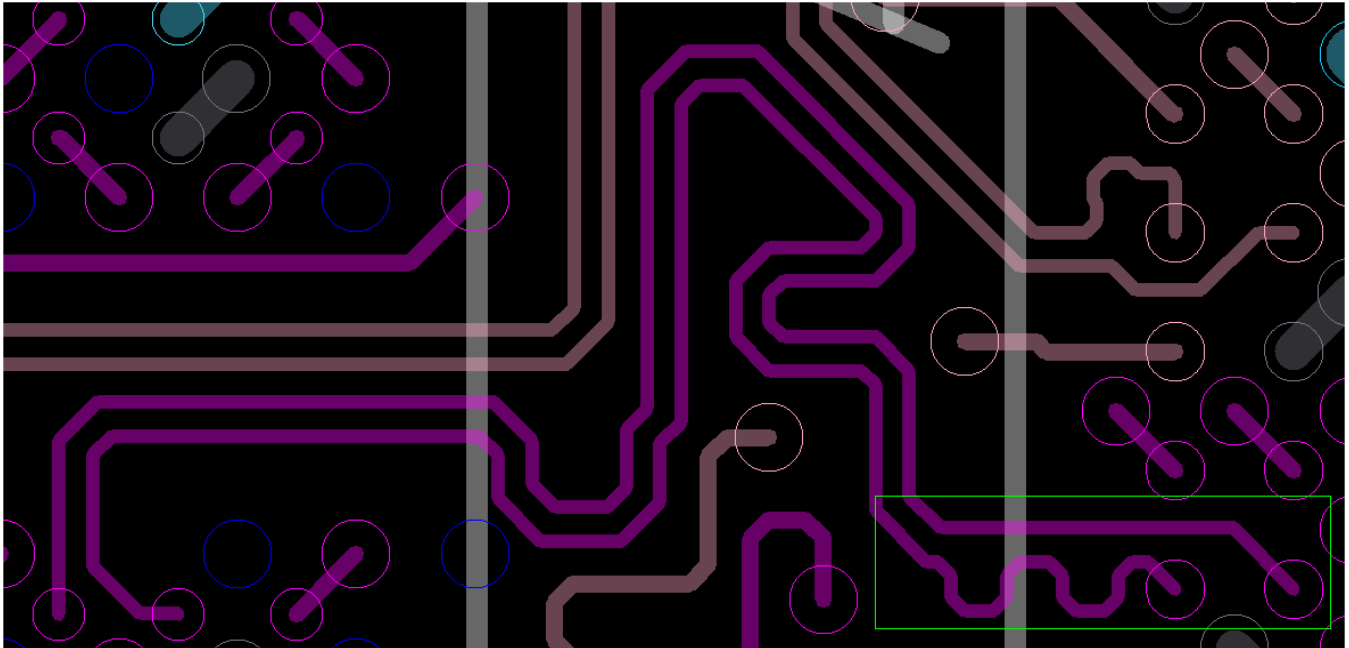


Figure 9. Small bumps added to the shorter differential pair

## 4. Avoiding board bring-up problems

### 4.1. Introduction

This chapter provides recommendations for avoiding typical mistakes when bringing up a board for the first time. These recommendations consist of basic techniques that have proven useful in the past for detecting board issues and addressing the three most typical bring-up pitfalls: power, clocks, and reset. A sample bring-up checklist is provided at the end of the chapter.

### 4.2. Using current monitor to avoid current pitfalls

Excessive current can damage the board. Avoid this problem by using a current-limiting laboratory supply set to the expected typical main current draw (at most). Monitor the main supply current with an ammeter when powering the board for the first time. The power supply's internal ammeter can be used (if it has one). By monitoring the main supply current and controlling the current limit, any excessive current can usually be detected before a permanent damage occurs.

### 4.3. Using current monitor to avoid voltage pitfalls

Using incorrect voltage rails is a common power pitfall. To avoid this mistake, create a basic table called "voltage report" before bringing up your board. This table helps you to validate that all the supplies are reaching the expected levels.

To create a voltage report, list the following:

- Board voltage sources.
- Default power-up values for the board voltage sources.
- The best location on the board to measure the voltage level of each supply.

Carefully determine the best measurement location for each power supply to avoid a large voltage drop (IR drop) on the board, which causes inaccurate current values to be measured. These guidelines help to produce the best current measurements:

- Measure as close to the load (in this case the i.MX 7ULP processor) as possible.
- Make two measurements: the first after the initial board power-up and the second while running a heavy use-case that stresses the i.MX 7ULP processor.

Ensure that the supplies that power the i.MX 7ULP meet the DC electrical specifications listed in the chip-specific data sheet.

**Table 20. Voltage report example**

Source	Net name	Expected (V)	Measured (V)	Measure point	Comment
Main	PSU_5V0	5.0		R39	
System 4.2 V	SYS_4V2	4.2		TP4	
PMIC Switcher 1	VDD_1V1	1.1		TP1	
PMIC Switcher 2	VDD_1V2	1.2		TP2	
PMIC Switcher 3	VDD_1V8	1.8		TP3	
PMIC LDO1	PMC_3V3	3.3			
PMIC LDO2	VDD_PTD	3.3/1.8			
PMIC LDO3	PMC_1V8	1.8			
SNVS	VDD_SNVS_3V0	3.0			
i.MX 7ULP	VDD_VBAT42	4.2			
i.MX 7ULP	VDD_DDR	1.2			
i.MX 7ULP	VDD_DIG1	1.1			
i.MX 7ULP	VDD_PMC18_DIG1	1.8			
i.MX 7ULP	VDD_PMC12_DIG0	1.2			
i.MX 7ULP	VDD18_DDR	1.8			
i.MX 7ULP	VDD_ANA33	3.3			
i.MX 7ULP	VDD_ANA18, VREFH_ANA18	1.8			
i.MX 7ULP	VDD_PMC18	1.8			
i.MX 7ULP	VDD_PMC11_DIG0_CAP	0.9			
i.MX 7ULP	VDD_PMC11_DIG1_CAP	1.05			
i.MX 7ULP	VDD_HSIC	1.2			
i.MX 7ULP	VDD_USB33	3.3			
i.MX 7ULP	VDD_USB18	1.8			
i.MX 7ULP	VDD18_IOREF	1.8			
i.MX 7ULP	VDD_DSI11	1.1			
i.MX 7ULP	VDD_DSI18	1.8			
i.MX 7ULP	VDD_PTA	3.3/1.8			
i.MX 7ULP	VDD_PTB	1.8			
i.MX 7ULP	VDD_PTC	3.3/1.8			
i.MX 7ULP	VDD_PTD	3.3/1.8			
i.MX 7ULP	VDD_PTE	3.3/1.8			
i.MX 7ULP	VDD_PTF	3.3/1.8			
i.MX 7ULP	DDR_VREF	0.6			

## 4.4. Checking for clock pitfalls

Problems with external clocks are another common source of board bring-up issues. Ensure that all your clock sources run as expected.

The EXTAL0/XTAL0 and EXTAL32/XTAL32 clocks are the main clock sources for the 24-MHz and 32-kHz reference clocks (respectively) on the i.MX 7ULP processor.

When checking crystal frequencies, use an active probe to avoid excessive loading. A parasitic probe prevents the 32.768-kHz and 24-MHz oscillators from starting up. Follow these guidelines:

- The EXTAL32 clock runs at 32.768 kHz (can be generated internally or applied externally).
- The EXTAL0/XTAL0 run at 24 MHz (used for the PLL reference).

## 4.5. Avoiding reset pitfalls

Follow these guidelines to ensure that the board boots in the correct boot mode.

- During the initial power-up, while asserting the RESET0\_b reset signal, ensure that the 24-MHz clock is active before releasing RESET0\_b.
- Follow the recommended power-up sequence specified in the i.MX 7ULP data sheet.
- Ensure that the RESET0\_b signal remains asserted (low) until all voltage rails associated with the boot-up are powered and stable.

The GPIOs and internal fuses control how the i.MX 7ULP processor boots. For more details about the different boot modes, see the “System boot” chapter of the chip reference manual.

## 4.6. Sample board bring-up checklist

Note that the checklist incorporates the recommendations described in the previous sections. The blank cells should be filled in during the bring-up.

**Table 21. Board bring-up checklist**

Checklist item	Details	Owner	Finding and status
<b>Note:</b> The following items must be completed serially.			
Perform a visual inspection.	Check the major components to make sure that nothing is misplaced or rotated before applying power.		
Verify all i.MX voltage rails.	Confirm that the voltages match the data sheet requirements. Be sure to check the voltages not only at the voltage source, but also as close to the i.MX processor as possible (such as on a bypass capacitor). This reveals any IR drops on the board that may cause issues later on. All the i.MX voltage rails should be checked.		
Verify the power-up sequence.	Verify that the power-on reset (RESET0_b) is de-asserted (high) after all power rails have come up and are stable. See the i.MX data sheet for details about the power-up sequencing.		
Measure/probe the input clocks (32 kHz, 24 MHz, and others).	Without a properly running clock, the i.MX does not function properly.		
Check the JTAG connectivity.	This is one of the most fundamental and basic access points to the i.MX to allow debugging		



**Table 21. Board bring-up checklist**

Checklist item	Details	Owner	Finding and status
	and execution of low-level code.		
<b>Note:</b> The following items may be worked on in parallel with the other bring-up tasks.			
Access the internal RAM.	Verify the basic operation of the i.MX processor in the system. Perform a basic test by performing a write-read-verify on the internal RAM. No software initialization is necessary to access the internal RAM.		
Measure the boot mode frequencies: <ul style="list-style-type: none"> <li>•Quad SPI (probe the slave select and measure the clock frequency).</li> <li>•eMMC/SD (measure the clock frequency).</li> </ul>	This verifies the specified signals' connectivity between the i.MX 7ULP processor and the boot device and that the boot mode signals are properly set. See the "System boot" chapter in the reference manual for details about configuring various boot modes.		
Run the basic DDR initialization and test the memory.	Assuming the use of a JTAG debugger, run the DDR initialization and open a debugger memory window pointing to the DDR memory map starting address. Try writing a few words and verify whether they are read correctly. If not, recheck the DDR initialization sequence and whether the DDR is correctly soldered onto the board. It is also recommended to recheck the schematic to ensure that the DDR memory is connected to the i.MX 7ULP processor correctly.		

## 5. IBIS model

The IBIS model for each i.MX processor is provided on the NXP website upon product release. Contact your local sales office or field applications engineer to check the availability of information before product releases.

The IBIS model filename indicates which package it applies to:

- The 10 mm x 10 mm "VK" package has "VK" in the filename.
- The 14 mm x 14 mm "VP" package has "VP" in the filename.

### 5.1. References

See these references for more information about the IBIS models and how they are used:

- IBIS Open Forum:  
The IBIS Open Forum consists of EDA vendors, computer manufacturers, semiconductor vendors, universities, and end-users. It proposes updates and reviews, revises standards, and organizes summits. It promotes the IBIS models and provides useful documentation and tools.
- IBIS specification.

## 6. Using BSDL for board-level testing

### 6.1. BSDL overview

The boundary scan description language (BSDL) is used for board-level testing after the components are assembled. The interface for this test uses the JTAG pins. The definition is contained within the IEEE standard 1149.1.

### 6.2. How BSDL works

The BSDL file defines the internal scan chain (which is the serial linkage of the IO cells) within a device. The scan chain looks like a large shift register which provides the means to read the logic level applied to a pin or to output a logic state on that pin. Using JTAG commands, the test tool uses the BSDL file to control the scan chain so that the device-board connectivity can be tested.

For example, when using an external ROM test interface, the test tool would do the following:

1. Output a specific set of addresses and controls to the pins connected to the ROM.
2. Perform a read command and scan out the values of the ROM data pins.
3. Compare the values read with the known golden values.

Based on this procedure, the tool can determine whether the interface between the two parts is connected properly and does not contain shorts or opens.

### 6.3. Downloading the BSDL file

The BSDL file for each i.MX processor is provided on the NXP website upon product release. Contact your local sales office or field applications engineer to check the availability of information before product releases.

### 6.4. Pin coverage of BSDL

Each pin is defined as a port within the BSDL file. Open the file using a text editor to review how each pin works. The BSDL file defines these functions:

- -- PORT DESCRIPTION TERMS.
- -- in = input only.
- -- out = 3-state output (0, Z, 1).
- -- buffer = 2-state output (0, 1).
- -- inout = bidirectional.
- -- linkage = OTHER (vdd, vss, analog).

The appearance of “linkage” in a pin’s definition implies that the pin cannot be used with the boundary scan. These are usually power pins or analog pins that cannot be defined with a digital logic state.

## 6.5. Boundary scan operation

See these references for more information:

- The “Secured JTAG controller (SJC)” chapter in the chip reference manual for the definitions of the JTAG interface operations.
- The “Fusemap” chapter in the chip reference manual for the fusemap tables.

## 7. Development platforms

This chapter provides a complete list of the development platforms that are available from NXP to support the i.MX 7ULP processors.

**Table 22. i.MX 7ULP EVK Revision B1**

Version of i.MX used	i.MX 7ULP.
<b>Schematic part number and revision</b>	170-29163 Revision B1 (EVK SOM board). 170-29164 Revision B1 (EVK base board).
<b>Features</b>	<p>SOM:</p> <ul style="list-style-type: none"> <li>• 1-GB LPDDR3.</li> <li>• 8-MB Quad SPI flash.</li> <li>• eMMC footprint.</li> <li>• Micro-SD 3.0 card socket.</li> <li>• USB 2.0 OTG with type C connector.</li> <li>• WiFi/Bluetooth.</li> <li>• PMIC NXP PF1550.</li> </ul> <p>Baseboard:</p> <ul style="list-style-type: none"> <li>• Full SD/MMC 3.0 card socket.</li> <li>• Audio codec and 3.5-mm audio jack.</li> <li>• 6-axis sensor with integrated linear accelerometer and magnetometer.</li> <li>• Gyroscope.</li> <li>• I<sup>2</sup>C precision pressure sensor with altimetry.</li> <li>• Arduino connector.</li> <li>• ADC/DAC connector.</li> <li>• Battery socket.</li> <li>• HDMI connector.</li> <li>• MIPI display panel connector.</li> <li>• MFI interface.</li> <li>• USB HSIC interface.</li> </ul>
<b>Quick start guide</b>	The quick start guide is available on the NXP website upon product release. Contact your local sales office or field applications engineer to check the availability of information before product releases.
<b>Schematic</b>	The schematic files are available on the NXP website upon product release. Contact your local sales office or field applications engineer to check the availability of information before product releases.
<b>Layout</b>	The layout files are available on the NXP website upon product release. Contact your local sales office or field applications engineer to check the availability of information before product releases.

**Table 23. i.MX 7ULP EVK Revision C0**

<b>Version i.MX used</b>	i.MX 7ULP.
<b>Schematic part number and revision</b>	170-38819 Revision C0 (EVK SOM board). 170-38818 Revision C0 (EVK base board).
<b>Features</b>	<p>SOM:</p> <ul style="list-style-type: none"> <li>• 1-GB LPDDR3.</li> <li>• 8-MB Quad SPI flash.</li> <li>• eMMC footprint.</li> <li>• Micro-SD 3.0 card socket.</li> <li>• USB 2.0 OTG with type C connector.</li> <li>• WiFi/Bluetooth (LBEE5KL1DX).</li> <li>• PMIC NXP PF1550.</li> </ul> <p>Baseboard:</p> <ul style="list-style-type: none"> <li>• Full SD/MMC 3.0 card socket.</li> <li>• Audio codec and 3.5-mm audio jack.</li> <li>• 6-axis sensor with integrated linear accelerometer and magnetometer.</li> <li>• Gyroscope.</li> <li>• I<sup>2</sup>C precision pressure sensor with altimetry.</li> <li>• Arduino connector.</li> <li>• ADC/DAC connector.</li> <li>• Battery socket.</li> <li>• HDMI connector.</li> <li>• MIPI display panel connector.</li> <li>• MFI interface.</li> <li>• USB HSIC interface.</li> </ul>
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