

i.MX 6SLL EVK Board Hardware User's Guide



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Chapter 1

Introduction

This hardware user's Guide is for i.MX 6SLL Evaluation Kit (EVK) based on the NXP Semiconductor i.MX 6SLL Applications Processor. The guide includes system setup and debugging, and provides detailed information on overall design and usage of the EVK board from a hardware systems perspective.

1.1 Board Overview

The EVK board is a platform designed to showcase the most commonly used features of the i.MX 6SLL Applications Processor in a small, low cost package.

The i.MX 6SLL EVK board is an entry level development board, which provides developer the option of becoming familiar with the processor before investing a large amount of resources in more specific designs.

The features of the i.MX 6SLL EVK board are shown in [Table 1](#)

Table 1. Board features		
Processor:	NXP Applications Processor	MCIMX6V7DVN10AB
DRAM Memory:	Micron 2GB LPDDR3	MT52L512M32D2PU-107 WT:B
Mass storage	MicroSD card connector	
	eMMC (unpopulated)	
Display interface	LCD connector	
USB	One USB host connector	
	One USB OTG connector	
Audio connectors:	3.5 mm Stereo Headphone output	
	Board-mounted microphone	
	Left & Right Speaker Out connectors(unpopulated)	
Power connector:	5 V DC-Jack	
Debug connectors:	UART to USB connector	
	20-pin JTAG connector(unpopulated)	
Bluetooth	20-pin Bluetooth Connector	
User Interface Buttons	Power Switch, ON/OFF, Reset button	
LED Indicators	Power status, UART	

Chapter 2 Specifications

This chapter provides detailed information about the electrical design and practical considerations of the EVK board and discuss each block of the following block diagram of the EVK board.

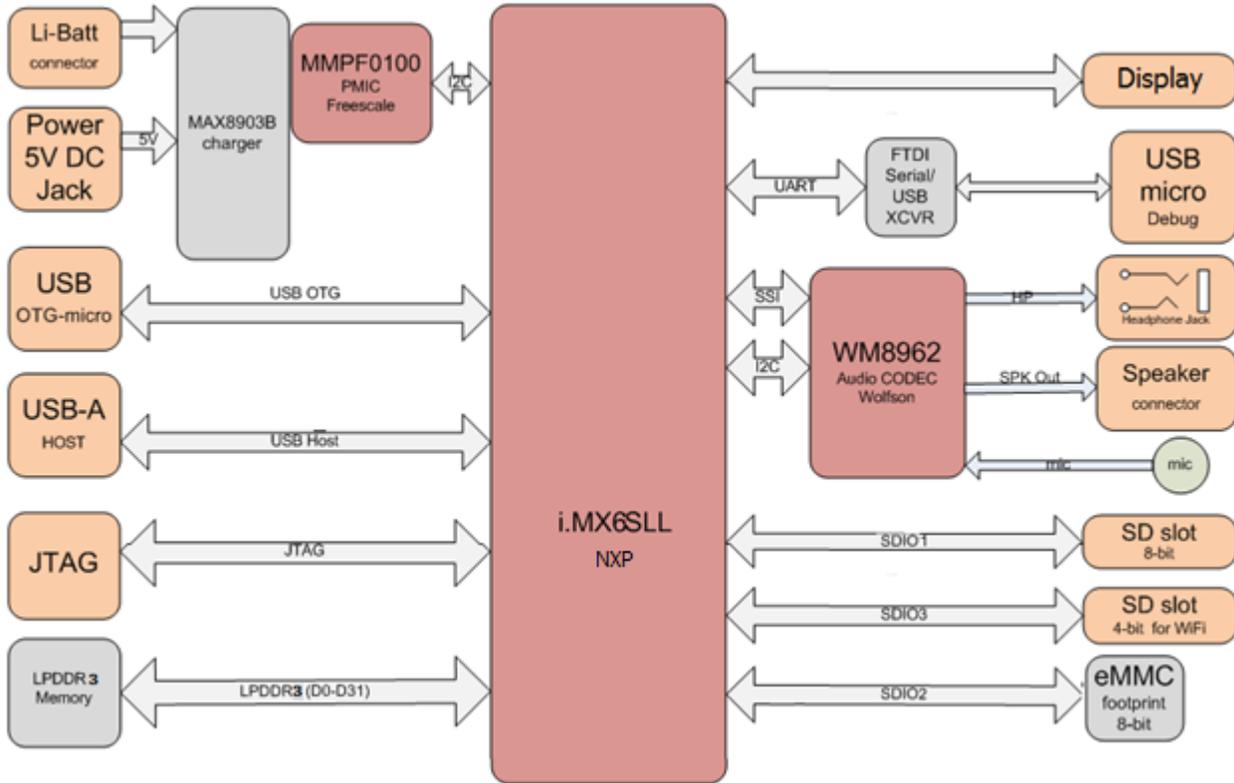


Figure 1. Block diagram

The overview of the i.MX 6SLL EVK board is shown in [Figure 2](#) and [Figure 3](#)

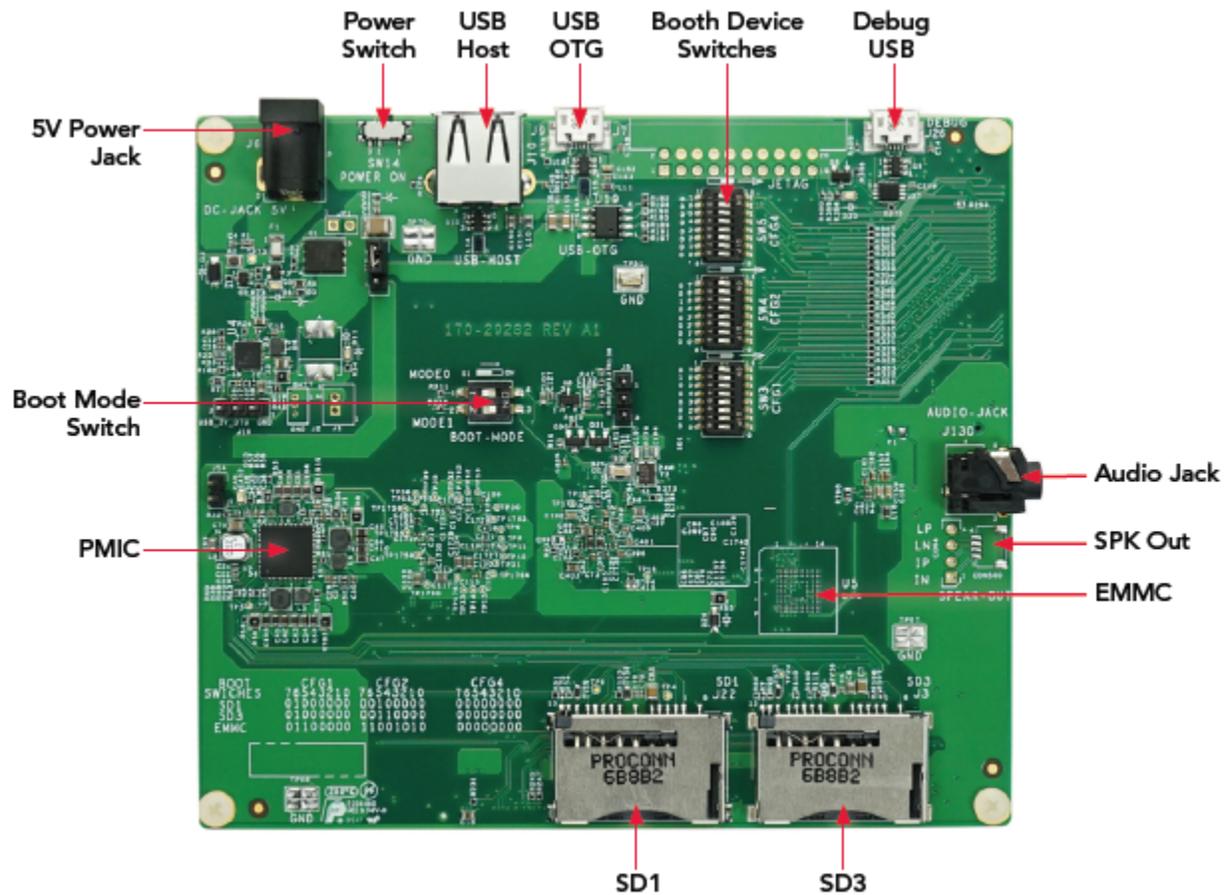


Figure 2. Front side of i.MX 6SLL EVK (top)

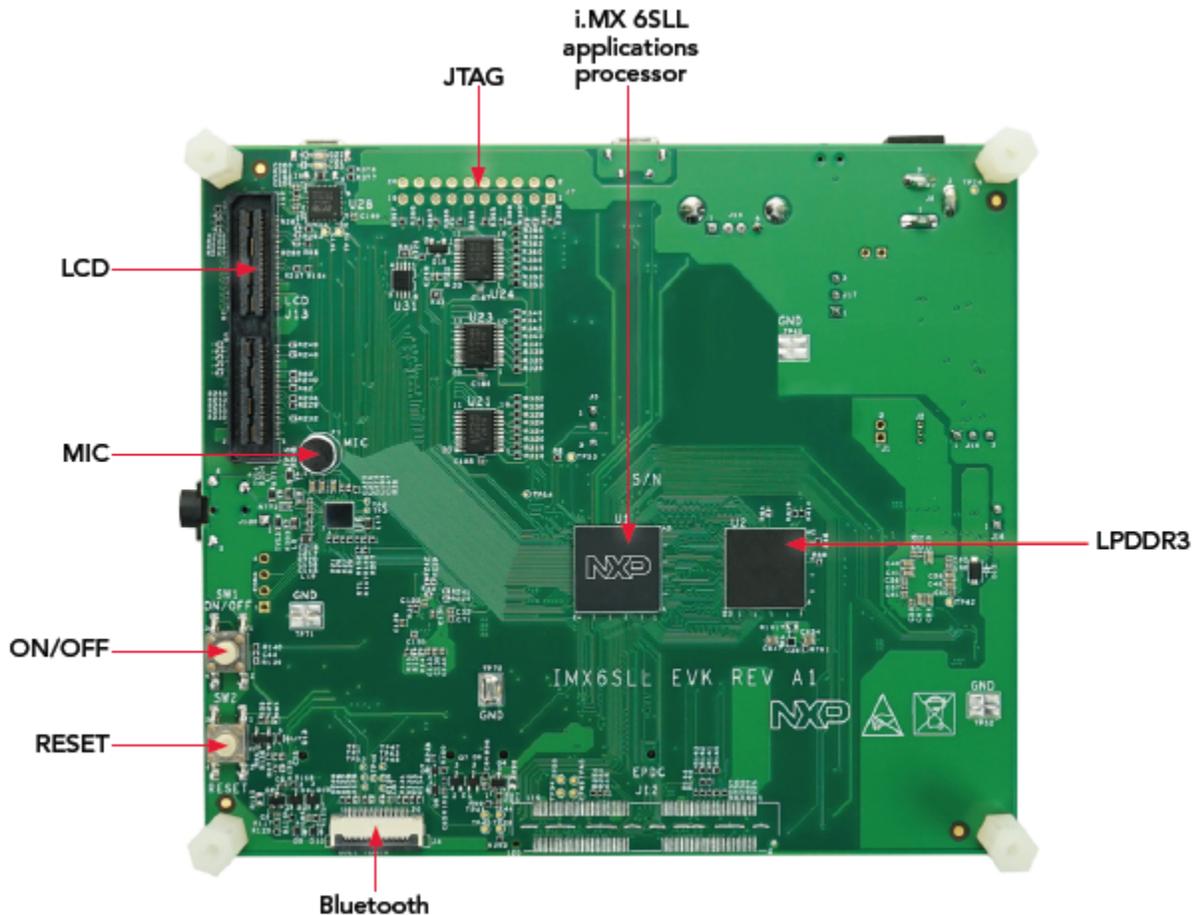


Figure 3. Back side of i.MX 6SLL EVK (bottom)

2.1 i.MX 6SLL processor

The i.MX 6SLL processor is the latest achievement of NXP in integrated multimedia applications processors, that offer high performance processing and optimized for lowest power consumption.

The processor features NXP's advanced implementation of a single ARM® Cortex®-A9, which operates at speed up to 1 GHz. The processor provides a 32-bit DDR interface that supports LPDDR2 and LPDDR3. In addition, there are number of other interfaces for connecting peripherals, such as WLAN, Bluetooth™, GPS, displays, and camera sensors.

More detailed information about the processor can be found in the data sheets i.MX 6SLL Applications Processors for Consumer Products (document [IMX6SLLCEC](#)), and the i.MX 6SLL Applications Processor Reference Manual (document [IMX6SLLRM](#)).

2.2 Boot mode configurations

BOOT_MODE [1:0] is used to select system boot mode. On i.MX 6SLL EVK board, a dual-switch (S1) is used to select the input voltage of these two pins, either 0 V or 3.3 V.

[Table 2](#) shows the switch configuration of boot mode for i.MX 6SLL EVK. Internal boot is chosen as default.

BOOT_MODE[1:0]	BOOT TYPE
00	Boot from fuses
01	Serial downloader
10	Internet boot
11	Reserved

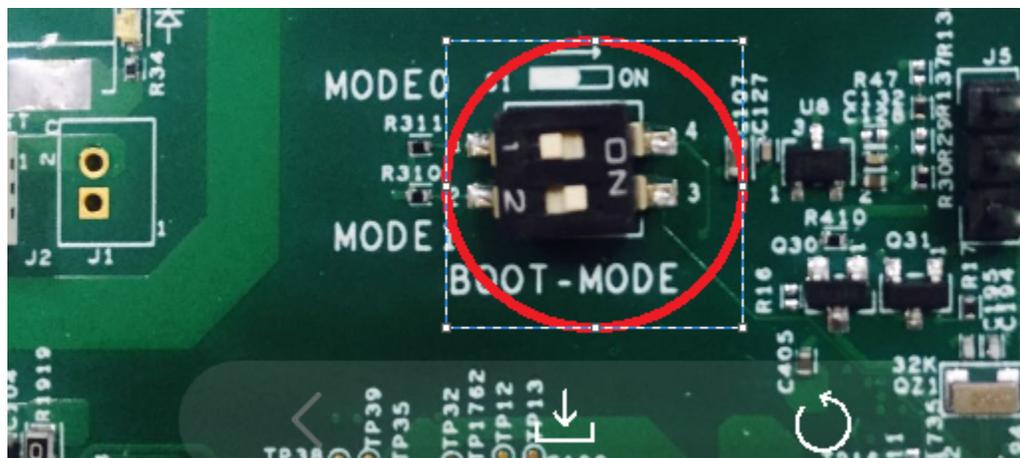


Figure 4. Boot mode settings

Table 3 shows the switch configuration of boot device for i.MX 6SLL EVK. SD1 is chosen as default.

BOOT SWITCHES	SW3 76543210	SW4 76543210	SW5 76543210
SD1	01000000	00100000	00000000
SD3	01000000	00110000	00000000
EMMC	01100000	11001010	00000000

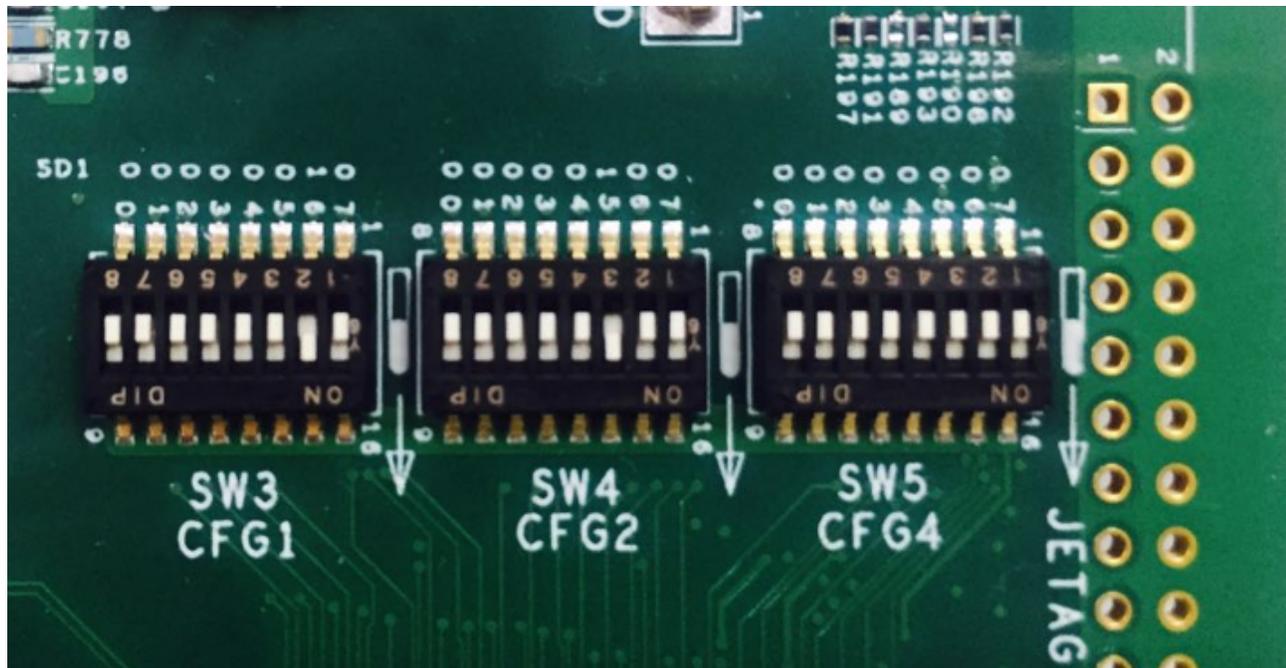


Figure 5. Boot device settings

NOTE

For more information about boot mode configuration, see the System Boot chapter of the i.MX 6SLL Reference Manual. For more information about i.MX 6SLL EVK boot device selection and configuration, see the board schematic.

2.3 Power tree

A DC 5 V/4A external power supply is used to supply the i.MX 6SLL EVK board at connector J6, and a slide switch SW14 is used to turn the power ON/OFF. There is an over-voltage protection circuit at the input power rail, so if the output voltage of the power supply exceeds 5.6 V, the circuit will shut the system down. Discrete regulators are used to generate different power rails for the whole system.

The power tree is shown in [Figure 6](#).

i.MX6SLL EVK PWR TREE

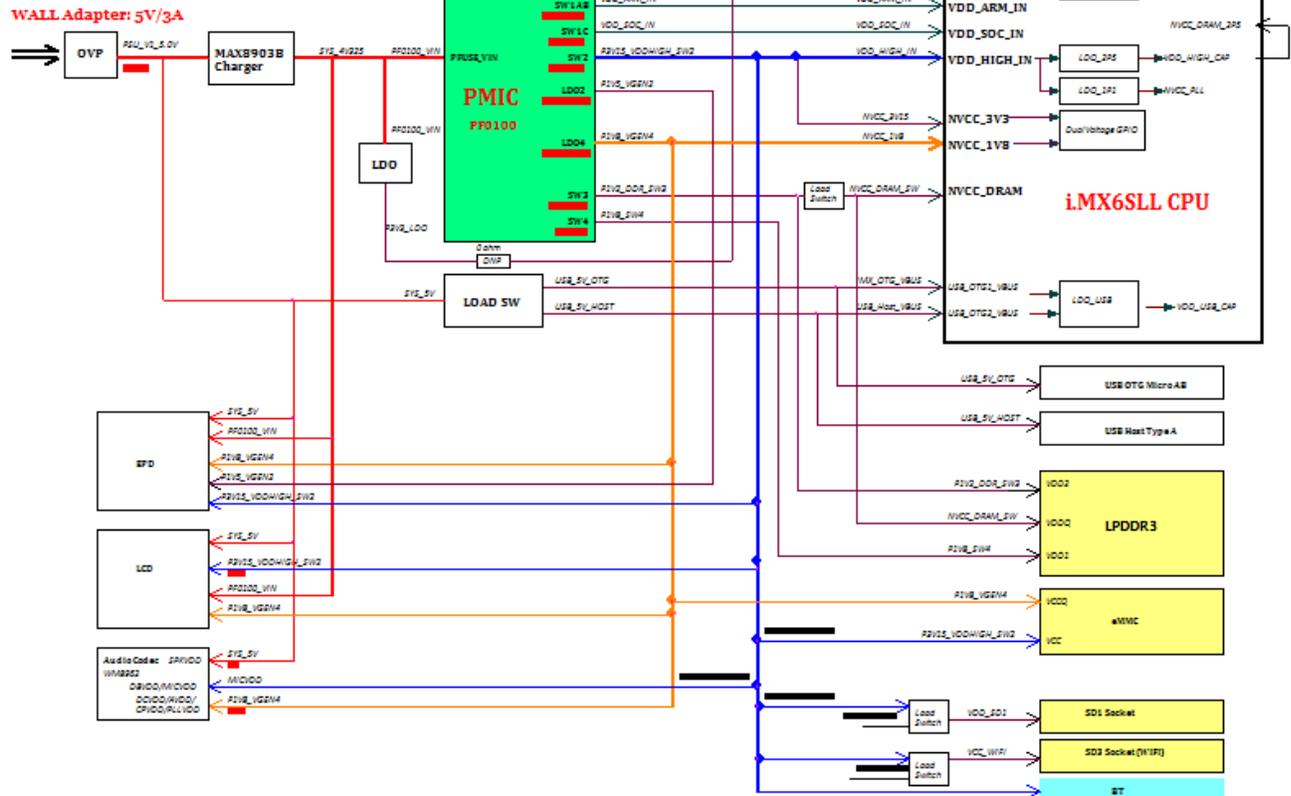


Figure 6. Power tree

The power tree displays all of the power supply rails used on the EVK board.

The power control logic of the i.MX 6SLL EVK board is shown in Figure 7.

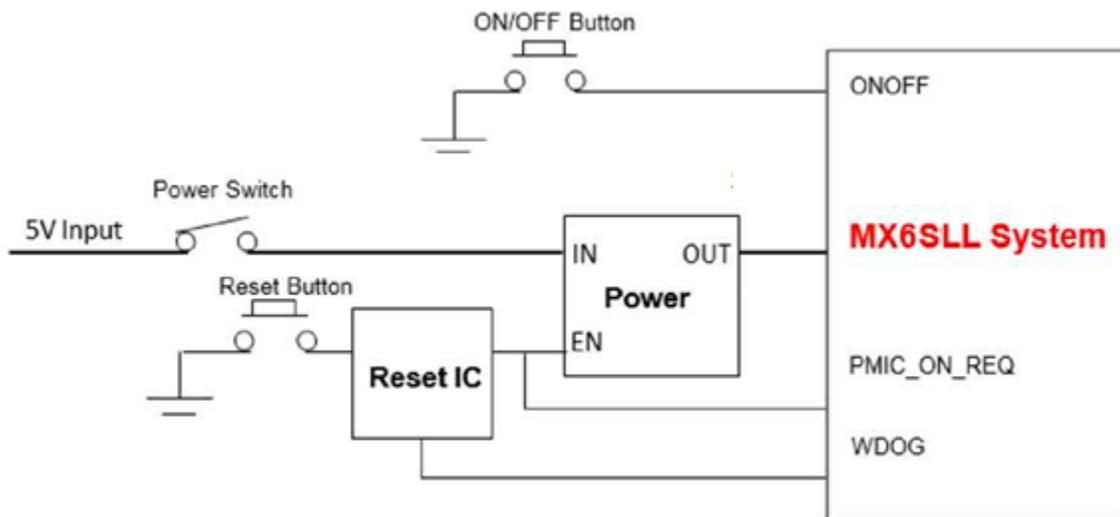


Figure 7. Power control diagram

The power rails on the board are shown in Table 4.

Table 4. PMIC output rails

PFUSE100	Voltage(V)	Current(A)	Power up sequence	Note
SW1A/B	1.2	2.5	2	
SW1C	1.2	1.7	2	
SW2	3.15	2	1	
SW3A/B	1.2	2.5	4	
SW4	1.8	1	3	
SWBST	5	0.6	6	
VGEN1	1.2	0.1	-	
VGEN2	1.5	0.25	7	
VGEN3	1.8	0.1	7	
VGEN4	1.8	0.35	3	
VGEN5	2.5	0.1	5	
VGEN6	2.8	0.2	7	LED
VSNVS	3	0.0004	0	
VREFDDR	0.6	0.01	4	

Table 5. i.MX6SLL Power table

i.MX6SLL Voltage Rail	Voltage(V)	Current(mA)	Generated By	Power up Sequence
VDD_ARM_IN	1.2	1100	P1V2_VDDARM_SW1 AB	2
VDD_SOC_IN	1.2	650	P1V2_VDDSOC_SW1 C	2
VDD_SNVS_IN	3	1	P3V0_STBY	0
VDD_SNVS_CAP			INTERNAL	
VDD_HIGH_IN	3.15	100	P3V15_VDDHIGH_S W2	1
VDD_HIGH_CAP	2.5		INTERNAL	
NVCC_3V3	3.15	280	P3V15_VDDHIGH_S W2	1
NVCC_1V8	1.8	150	P1V8_VGEN4	3
VDD_PLL_CAP	1.1		INTERNAL	
VDD_USB_CAP	3		INTERNAL	
DARM_PWR_2P5	2.5		VDD_HIGH_CAP	

Table continues on the next page...

Table 5. i.MX6SLL Power table (continued)

DRAM_PWR	1.2	200	P1V2_DDR_SW3	4
DRAM_VREF	0.6	1	P0V6_VREFDDR	4

2.4 LPDDR3 SDRAM memory

The i.MX 6SLL EVK board has one 512 Meg x 32 LPDDR3 SDRAM (MT52L512M32D2PU-107 WT:B) for a total of 2GB memory.

The DDR_VREF is created by PMIC PF0100. The calibration resistors used by the LPDDR3 chips and the processor are 240 Ohm 1 % resistors. These resistor values are specified by the LPDDR3 specifications.

2.5 SD card slots (J3, J22)

There are two SD card connectors (J3, J22) on the i.MX 6SLL EVK board.

- J22 is for Boot.
- J3 can also support accessories such as a WiFi card, and so on.

2.6 eMMC

The eMMC interface is connected to USDHC2 of i.MX 6SLL. It can support up to eMMC 5.0, the eMMC device is not populated by default on the EVK board. To boot from eMMC, populate the eMMC device, and then change the boot device switch settings. The BOOT_CFG settings must be adjusted for the specified eMMC device. See [Table 3](#) for more information.

2.7 USB PHY connector (J9, J10)

The i.MX 6SLL Applications Processors contains two high speed (HS) USB 2.0 OTG (Up to 480 Mbps) controllers, with integrated HS USB Phy. On the EVK board, J10 is a Type-A connector for USB host port, J9 is a Micro-AB connector for USB OTG port. The OTG port J9 is also used for downloading the boot image by MFGTool in Serial Download Mode.

2.8 Audio input/output connectors (J130/P1/CON4 & CON500)

The Audio CODEC used on the i.MX 6SLL EVK board is Wolfson's Low Power, high quality Stereo Codec, WM8962. The digital interface between i.MX 6SLL and WM8962 includes four signals:

- LRCLK
- BCLK
- DACDAT
- ADCDAT

Specifications

i.MX 6SLL also provides the MCLK to WM8962.

i.MX 6SLL EVK includes one headphone interface (J130), one onboard MIC (P1), and speaker interfaces (CON4&CON500). J130 is a phone jack, which supports jack detect.

2.9 USB debug connector (J26)

On the EVK board, FT232RQ, a USB to Serial UART IC is used to convert the UART signal to the USB signal. With the Micro-B USB connector J26, the connection for debugging is simplified.

UART1 port is used as the default debug port. No RTS or CTS signals are sent from the processor to the debug connector because these signals are commonly ignored by most applications. The required terminal settings are shown in [Table 6](#).

Table 6. Terminal settings	
Baud rate	115,200
Data bits	8
Parity	None
Stop bits	1
Flow control	None

2.10 Bluetooth Connector (J4)

On the EVK board, the J4 is connected to i.MX 6SLL UART5 port, and can be used for Bluetooth. Silex Bluetooth module SX-SDCAN-2830BT is recommended. To verify other Bluetooth modules, a convert board may be needed.

NOTE

J4 is a bottom-contact type connector for BT connection on the EVK board. 20-pin/0.5 mm pitch same side FFC/FPC should be used to connect with Silex Bluetooth module SX-SDCAN-2830BT.

2.11 JTAG connector (J7, unpopulated)

J7 is a standard 20-pin/2.54 mm Box Header Connector for JTAG. The pin definitions are shown in the following figure. JTAG is not populated by default on the EVK board.

JTAG

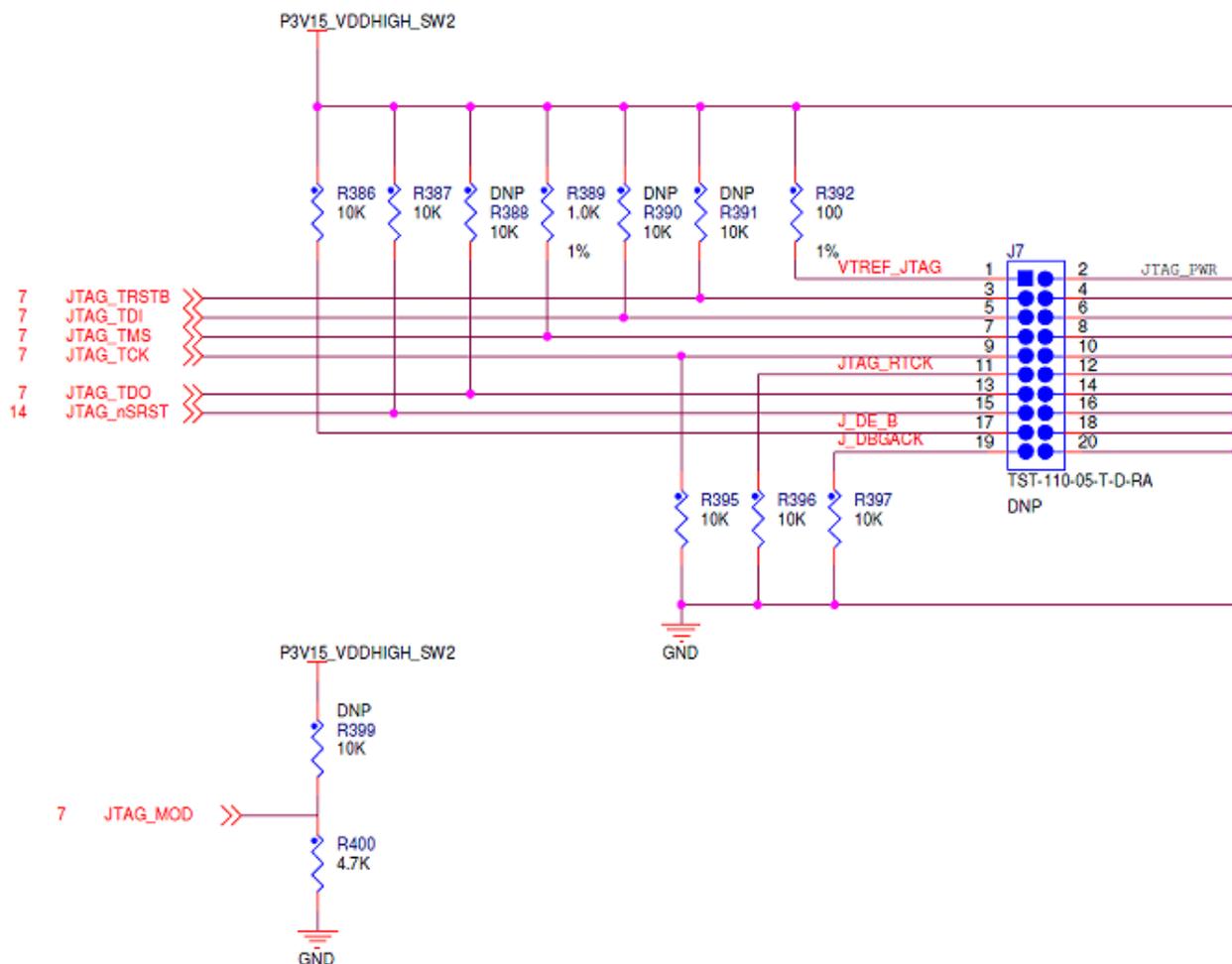


Figure 8. JTAG pin definitions

2.12 User interface switches

There are jumpers, push button and switches on the EVK board. Their functionality is listed in [Table 7](#).

Reference	Shunt Installation	Function
J16	1-2	Use cable to pins 1 and 2 to connect an external charger
	2-3	Shunt 2-3 to experiment with USB charging

Table continues on the next page...

Table 7. Switches function (continued)

Reference	Shunt Installation	Function
	OpenD	No charger
J17	1-2	5 V rail supplied by PMIC (600 mA limited)
	2-3	5 V rail supplied from wall adapter
J14	1-2	Connect the coin cell if needed
	OpenD	
SW14	Evaluation kit switch <ul style="list-style-type: none"> Sliding the switch to the ON position connects the 5 V power supply to the Evaluation kit main power system. Sliding the switch to the OFF position immediately removes all power from the board. 	
SW1	Evaluation kit ON/OFF button <ul style="list-style-type: none"> Prolonged depress (>5 sec) will force an immediate hardware shutdown. If board is in the SHUTDOWN state, short press of the button will restart (boot) the system. If board is in the STANDBY state, short press of the button will bring the system out of standby (resume operation, no boot). 	
SW2	Evaluation kit RESET button <ul style="list-style-type: none"> Press of the button will reset the system and begin a boot sequence. 	

2.13 User interface LED indicators

There are two LED status indicators located on the board. The functions of these LEDs include:

- Main Power Supply (D11)
—Green: The input of PMIC IC PF0100 is normal.
- PMIC ON (D15)
—Green: The output of PMIC IC PF0100 is normal.
- Over voltage (D6)
—Red: WALL—5V—DC—JACK is over 5.6 V
- UART (D21,D22)
—Red flashing (D21): Debug UART data are being transmitted to PC.
—Green flashing (D22): Debug UART data are being received from PC.

2.14 Optional back-up coin cell holder (J14)

On the i.MX 6SLL EVK board, there is a connector (J14) for holding a Lithium coin cell battery. The coin cell provides an alternative power supply for i.MX 6SLL VDD_SNVS_IN power rail when the main P3V15_VDDHIGH_SW2 is off. The i.MX 6SLL has an internal LDO to regulate the VDD_SNVS_CAP power to supply the RTC subsystem. When DC 5 V power supply is removed, the coin cell will provide power only to the VDD_SNVS_IN power rail of the EVK board. To increase the keep time of RTC, the developer should optimize the power consumption of the whole VDD_SNVS_IN power rail.

2.15 LCD daughter card(J13)

If developers want to use LCD, NXP provides an optional LCD daughter card MCIMX28LCD, which has to be connected to J13. For more information about this board, please visit www.nxp.com

2.16 EPDC expansion port (J12,unpopulated)

EPDCsupport via EPD daughterboard X-IMXEBOOKDC4,which has to be connec ted to J12 (SAMTEC , QSH-060-01-L-D-A), J12 is unpopulated on 6SLL EVK. For more information about EPD daughter board, please visit www.nxp.com.

Chapter 3

PCB Information

The EVK board are made using standard 6-layer technology. The material used was FR-4.

The PCB stack-up information is shown in [Figure 9](#).

	Subclass Name	Type	Thickness (MIL)	Dielectric Constant	Loss Tangent	Negative Artwork	Shield	Width (MIL)	Coupling Type	Spacing (MIL)	DiffZ0 (ohm)
1		SURFACE		1	0						
2		DIELECTRIC	0.4	3.5	0						
3	TOP	CONDUCTOR	1.7	1	0	<input type="checkbox"/>		4.00	EDGE	4.00	86.92
4		DIELECTRIC	2.5	4	0.035						
5	L2_GND_1	PLANE	1.2	1	0	<input type="checkbox"/>	<input checked="" type="checkbox"/>				
6		DIELECTRIC	3	4	0.035						
7	L3_IN1	CONDUCTOR	1.2	1	0	<input type="checkbox"/>		3.50	EDGE	5.50	96.416
8		DIELECTRIC	42	3.5	0.035						
9	L4_POWER	PLANE	1.2	1	0	<input type="checkbox"/>	<input checked="" type="checkbox"/>				
10		DIELECTRIC	3	4	0.035						
11	L5_GND_2	PLANE	1.2	1	0	<input type="checkbox"/>	<input checked="" type="checkbox"/>				
12		DIELECTRIC	2.5	4	0.035						
13	BOTTOM	CONDUCTOR	1.7	1	0	<input type="checkbox"/>		3.50	EDGE	5.50	97.099
14		DIELECTRIC	0.4	3.5	0						
15		SURFACE		1	0						

Figure 9. Board stack-up information

Chapter 4

EVK Design Files

The schematics, layout files, and gerber files (including Silkscreen) can be downloaded from www.nxp.com/IMX6SLEVK

Chapter 5

Contents of the Evaluation Kit

Table 8. EVK contents

Item	Description
Board	MCIMX6SLLEVK
USB Cable	USB AM TO MICRO USB 5P 1.0M
Documentation	Quick Start Guide
Power supply	100/240 V input, 5 V, 4 A output
SD card	containing Linux OS

Chapter 6

References

The following references can be found on www.nxp.com

1. i.MX 6SLL Applications Processor Reference Manual (document [IMX6SLLRM](#))
2. i.MX 6SLL Applications Processors for Consumer Products (document [IMX6SLLCEC](#))

Chapter 7

Revision History

Table 9. Revision history

Revision number>	Date	Substantive changes
0	06/2017	Initial release

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