

GigaDevice Semiconductor Inc.

GD32F101xx

ARM® Cortex™ -M3 32-bit MCU

Datasheet

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1. General description

The GD32F101xx device is a 32-bit general-purpose microcontroller based on the ARM® Cortex™-M3 RISC core with best ratio in terms of processing power, reduced power consumption and peripheral set. The Cortex™-M3 is a next generation processor core which is tightly coupled with a Nested Vectored Interrupt Controller (NVIC), SysTick timer and advanced debug support.

The GD32F101xx device incorporates the ARM® Cortex™-M3 32-bit processor core operating at 56 MHz frequency with Flash accesses zero wait states to obtain maximum efficiency. It provides up to 3 MB on-chip Flash memory and up to 80 KB SRAM memory. An extensive range of enhanced I/Os and peripherals connected to two APB buses. The devices offer up to two 12-bit ADCs, up to ten general 16-bit timers and two basic timers, as well as standard and advanced communication interfaces: up to three USARTs, two UARTs, three SPIs and two I2Cs.

The device operates from a 2.6 to 3.6 V power supply and available in –40 to +85 °C temperature range. Several power saving modes provide the flexibility for maximum optimization between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features make the GD32F101xx devices suitable for a wide range of applications, especially in areas such as industrial control, user interface, power monitor and alarm systems, consumer and handheld equipment, touch panel, PC peripherals and so on.



2. Device overview

2.1. Device information

Table 2-1. GD32F101xx devices features and peripheral list

| Part Number | GD32F101xx | | | | | | | | | | | | | |
|---------------------|------------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|---------------------------|
| | T4 | T6 | T8 | TB | C4 | C6 | C8 | CB | R4 | R6 | R8 | RB | V8 | VB |
| Flash (KB) | 16 | 32 | 64 | 128 | 16 | 32 | 64 | 128 | 16 | 32 | 64 | 128 | 64 | 128 |
| SRAM (KB) | 4 | 6 | 10 | 16 | 4 | 6 | 10 | 16 | 4 | 6 | 10 | 16 | 10 | 16 |
| Timers | General timer(16-bit) | 2 <small>(1-2)</small> | 2 <small>(1-2)</small> | 3 <small>(1-3)</small> | 3 <small>(1-3)</small> | 2 <small>(1-2)</small> | 2 <small>(1-2)</small> | 3 <small>(1-3)</small> | 3 <small>(1-3)</small> | 2 <small>(1-2)</small> | 2 <small>(1-2)</small> | 3 <small>(1-3)</small> | 3 <small>(1-3)</small> | 3 <small>(1-3)</small> |
| | SysTick | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Watchdog | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| | RTC | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Connectivity | USART | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> |
| | I2C | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> |
| | SPI | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> |
| GPIO | 26 | 26 | 26 | 26 | 37 | 37 | 37 | 37 | 51 | 51 | 51 | 51 | 80 | 80 |
| EXMC | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| EXTI | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 |
| ADC | Units | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> |
| | Channels | 10 | 10 | 10 | 10 | 10 | 10 | 10 | 10 | 16 | 16 | 16 | 16 | 16 |
| Package | QFN36 | | | | LQFP48 | | | | LQFP64 | | | | LQFP100 | |

Table 2-2. GD32F101xx devices features and peripheral list (continued)

| Part Number | | GD32F101xx | | | | | | | | | | | | | | |
|---------------------|------------------------------|---------------------------|---------------------------|---------------------------|---------------------------------|---------------------------------|---------------------------------|---------------------------------|---------------------------|---------------------------|---------------------------|---------------------------------|---------------------------------|---------------------------------|---------------------------------|---------------------------|
| | | RC | RD | RE | RF | RG | RI | RK | VC | VD | VE | VF | VG | VI | VK | |
| Flash (KB) | | 256 | 384 | 512 | 768 | 1024 | 2048 | 3072 | 256 | 384 | 512 | 768 | 1024 | 2048 | 3072 | |
| SRAM (KB) | | 32 | 48 | 48 | 80 | 80 | 80 | 80 | 32 | 48 | 48 | 80 | 80 | 80 | 80 | |
| Timers | General timer(16-bit) | 4 <small>(1-4)</small> | 4 <small>(1-4)</small> | 4 <small>(1-4)</small> | 10 <small>(1-4,8-13)</small> | 10 <small>(1-4,8-13)</small> | 10 <small>(1-4,8-13)</small> | 10 <small>(1-4,8-13)</small> | 4 <small>(1-4)</small> | 4 <small>(1-4)</small> | 4 <small>(1-4)</small> | 10 <small>(1-4,8-13)</small> | 10 <small>(1-4,8-13)</small> | 10 <small>(1-4,8-13)</small> | 10 <small>(1-4,8-13)</small> | |
| | SysTick | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |
| | Basic timer(16-bit) | 2 <small>(5-6)</small> | 2 <small>(5-6)</small> | 2 <small>(5-6)</small> | 2 <small>(5-6)</small> | 2 <small>(5-6)</small> | 2 <small>(5-6)</small> | 2 <small>(5-6)</small> | 2 <small>(5-6)</small> | 2 <small>(5-6)</small> | 2 <small>(5-6)</small> | 2 <small>(5-6)</small> | 2 <small>(5-6)</small> | 2 <small>(5-6)</small> | 2 <small>(5-6)</small> | 2 <small>(5-6)</small> |
| | Watchdog | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| | RTC | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Connectivity | USART | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | |
| | UART | 2 <small>(3-4)</small> | 2 <small>(3-4)</small> | 2 <small>(3-4)</small> | 2 <small>(3-4)</small> | 2 <small>(3-4)</small> | 2 <small>(3-4)</small> | 2 <small>(3-4)</small> | 2 <small>(3-4)</small> | 2 <small>(3-4)</small> | 2 <small>(3-4)</small> | 2 <small>(3-4)</small> | 2 <small>(3-4)</small> | 2 <small>(3-4)</small> | 2 <small>(3-4)</small> | 2 <small>(3-4)</small> |
| | I2C | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> |
| | SPI | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> |
| GPIO | | 51 | 51 | 51 | 51 | 51 | 51 | 51 | 80 | 80 | 80 | 80 | 80 | 80 | 80 | 80 |
| EXMC | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| EXTI | | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 |
| ADC | Units | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> | |
| | Channels | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 |
| Package | | LQFP64 | | | | | | | LQFP100 | | | | | | | |

Table 2-3. GD32F101xx devices features and peripheral list (continued)

| Part Number | | GD32F101xx | | | | | | |
|--------------|-----------------------|---------------------------|---------------------------|---------------------------|---------------------------------|---------------------------------|---------------------------------|---------------------------------|
| | | ZC | ZD | ZE | ZF | ZG | ZI | ZK |
| Flash (KB) | | 256 | 384 | 512 | 768 | 1024 | 2048 | 3072 |
| SRAM (KB) | | 32 | 48 | 48 | 80 | 80 | 80 | 80 |
| Timers | General timer(16-bit) | 4 <small>(1-4)</small> | 4 <small>(1-4)</small> | 4 <small>(1-4)</small> | 10 <small>(1-4,8-13)</small> | 10 <small>(1-4,8-13)</small> | 10 <small>(1-4,8-13)</small> | 10 <small>(1-4,8-13)</small> |
| | SysTick | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Basic timer(16-bit) | 2 <small>(5-6)</small> | 2 <small>(5-6)</small> | 2 <small>(5-6)</small> | 2 <small>(5-6)</small> | 2 <small>(5-6)</small> | 2 <small>(5-6)</small> | 2 <small>(5-6)</small> |
| | Watchdog | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| | RTC | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Connectivity | USART | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> |
| | UART | 2 <small>(3-4)</small> | 2 <small>(3-4)</small> | 2 <small>(3-4)</small> | 2 <small>(3-4)</small> | 2 <small>(3-4)</small> | 2 <small>(3-4)</small> | 2 <small>(3-4)</small> |
| | I2C | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> |
| | SPI | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> | 3 <small>(0-2)</small> |
| GPIO | | 112 | 112 | 112 | 112 | 112 | 112 | 112 |
| EXMC | | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| EXTI | | 16 | 16 | 16 | 16 | 16 | 16 | 16 |
| ADC | Units | 1 <small>(0)</small> | 1 <small>(0)</small> | 1 <small>(0)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> | 2 <small>(0-1)</small> |
| | Channels | 16 | 16 | 16 | 16 | 16 | 16 | 16 |
| Package | | LQFP144 | | | | | | |

2.2. Block diagram

Figure 2-1. GD32F101x4/6/8/B block diagram

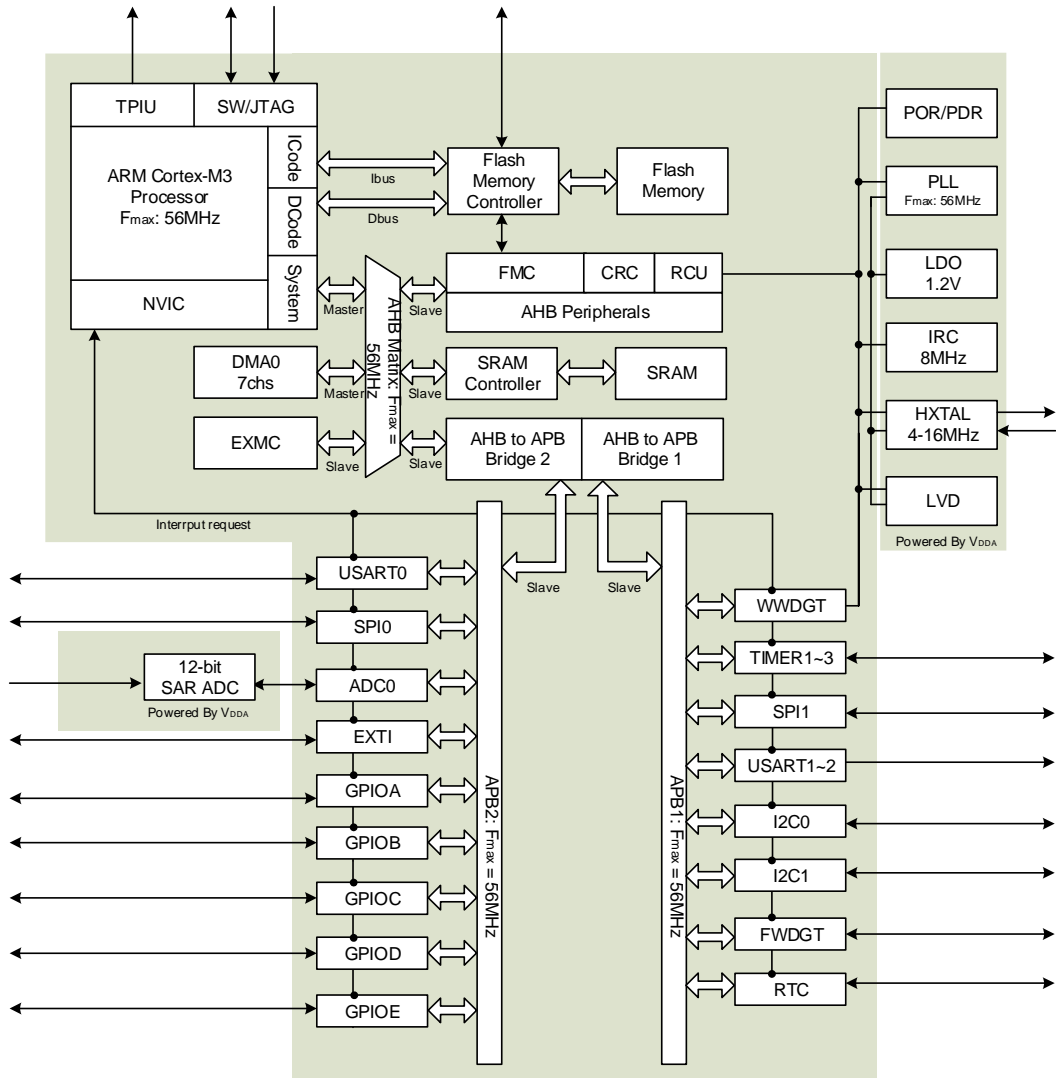
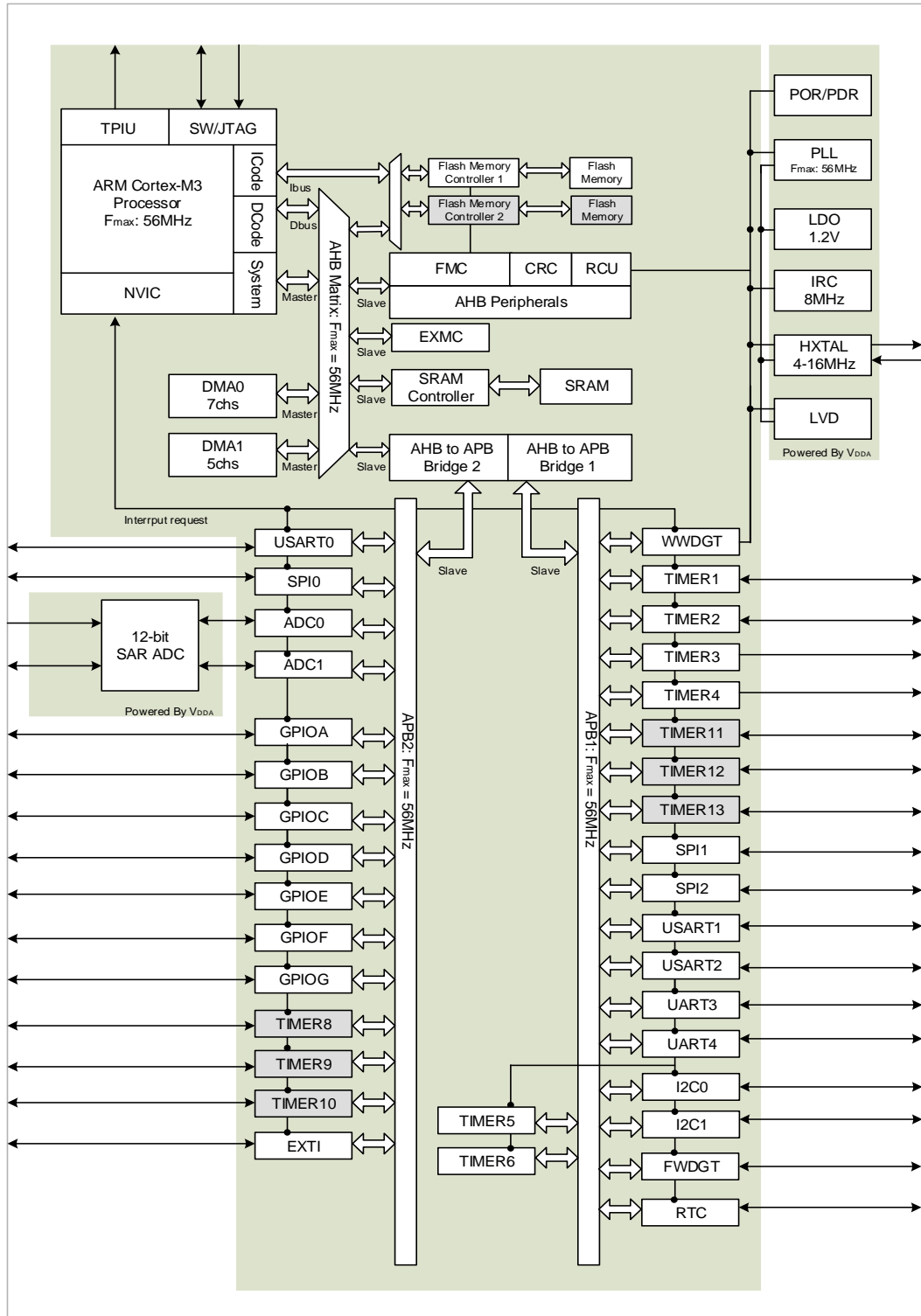


Figure 2-2. GD32F101xC/D/E/F/G/I/K block diagram



☐: Blocks are available in GD32F101xF/G/I/K devices

2.3. Pinouts and pin assignment

Figure 2-3. GD32F101Zx LQFP144 pinouts

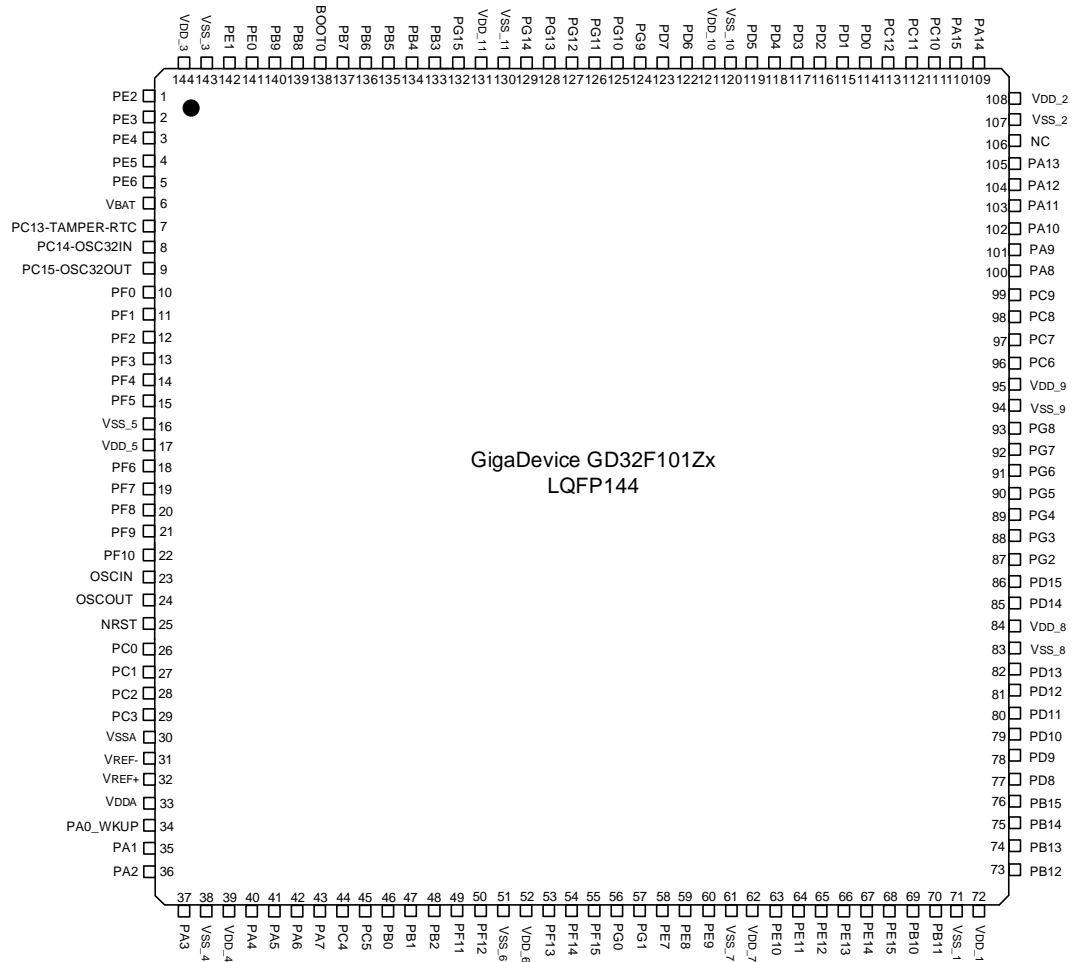


Figure 2-4. GD32F101Vx LQFP100 pinouts

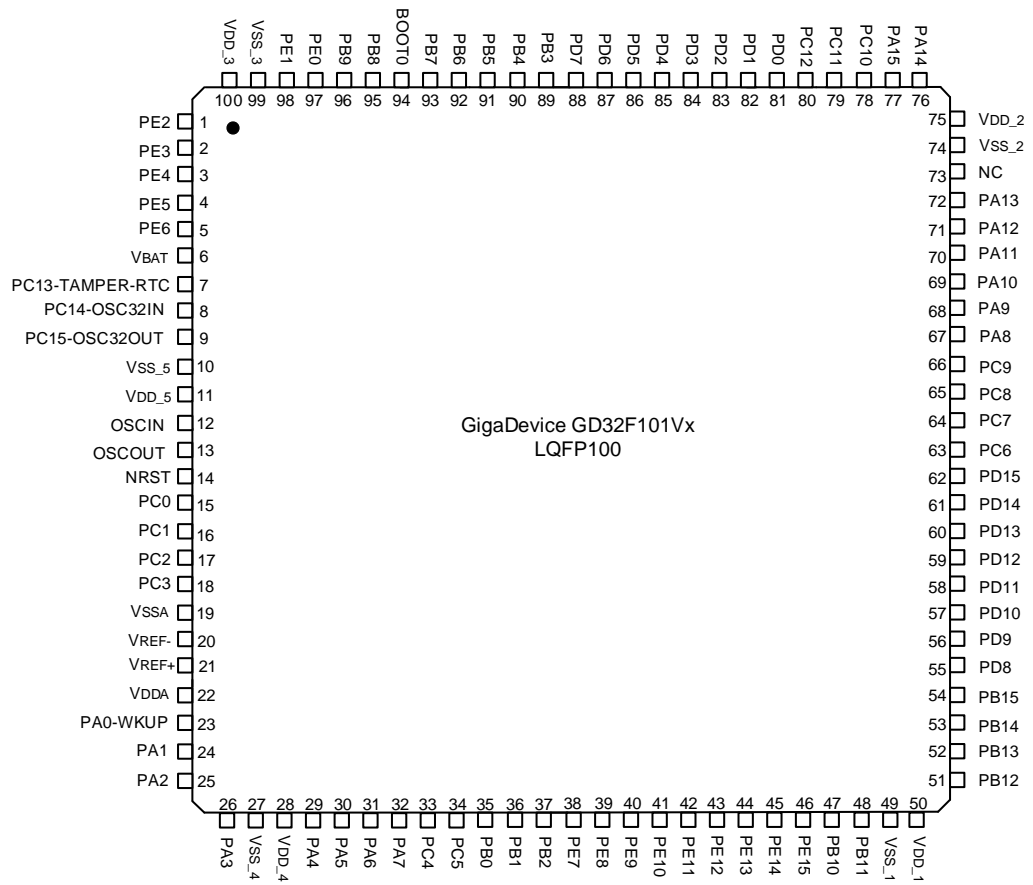


Figure 2-5. GD32F101Rx LQFP64 pinouts

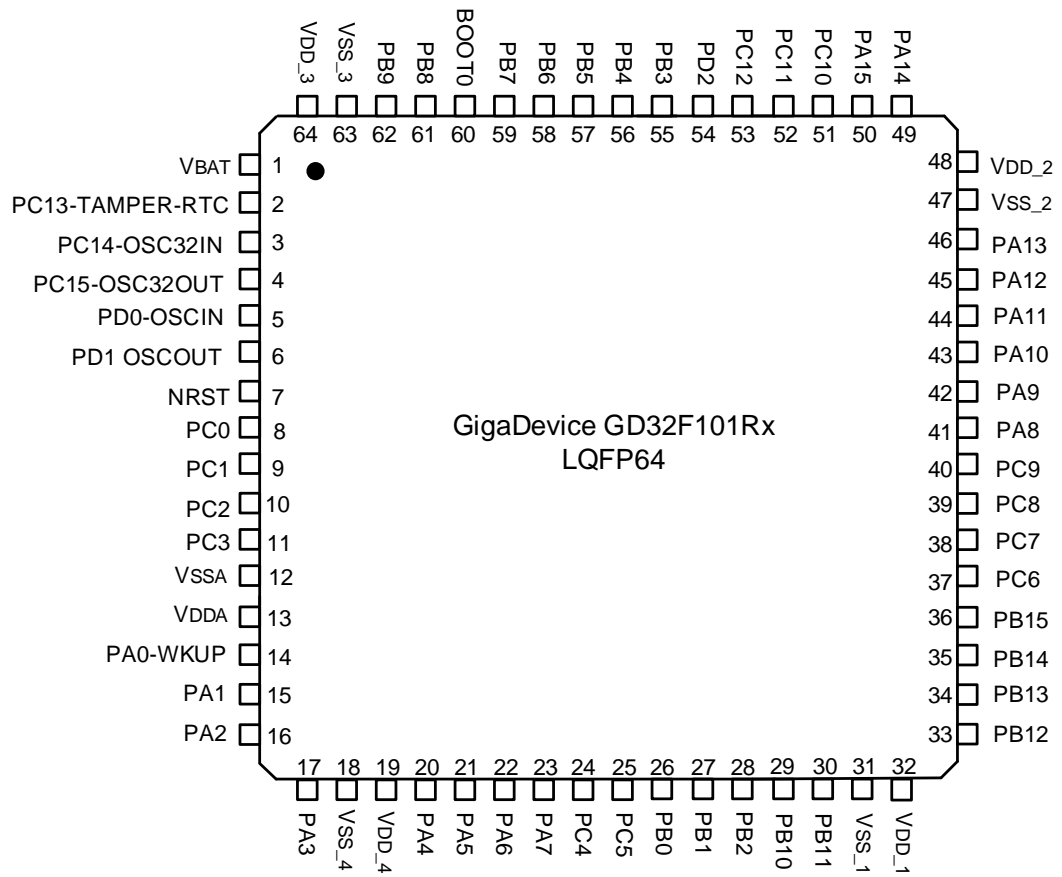


Figure 2-6. GD32F101Cx LQFP48 pinouts

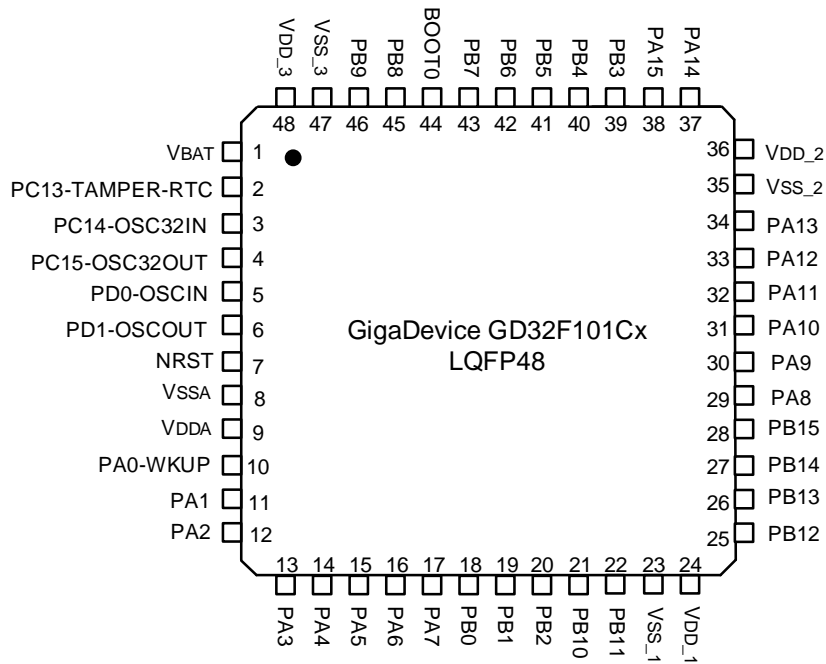
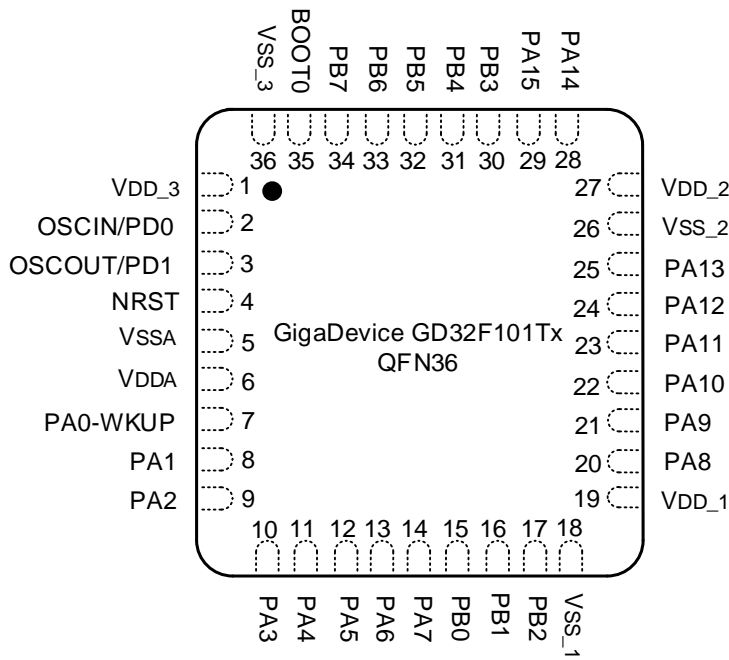


Figure 2-7. GD32F101Tx QFN36 pinouts



2.4. Memory map

Table 2-4. GD32F101xx memory map

| Pre-defined Regions | Bus | Address | Peripherals |
|---------------------|-----|---------------------------|-----------------------|
| External device | AHB | 0xA000 0000 - 0xA000 0FFF | EXMC - SWREG |
| External RAM | | 0x9000 0000 - 0x9FFF FFFF | EXMC - PC CARD |
| | | 0x7000 0000 - 0x8FFF FFFF | EXMC - NAND |
| | | 0x6000 0000 - 0x6FFF FFFF | EXMC - NOR/PSRAM/SRAM |
| Peripheral | AHB | 0x5000 0000 - 0x5003 FFFF | Reserved |
| | | 0x4008 0000 - 0x4FFF FFFF | Reserved |
| | | 0x4004 0000 - 0x4007 FFFF | Reserved |
| | | 0x4002 BC00 - 0x4003 FFFF | Reserved |
| | | 0x4002 B000 - 0x4002 BBFF | Reserved |
| | | 0x4002 A000 - 0x4002 AFFF | Reserved |
| | | 0x4002 8000 - 0x4002 9FFF | Reserved |
| | | 0x4002 6800 - 0x4002 7FFF | Reserved |
| | | 0x4002 6400 - 0x4002 67FF | Reserved |
| | | 0x4002 6000 - 0x4002 63FF | Reserved |
| | | 0x4002 5000 - 0x4002 5FFF | Reserved |
| | | 0x4002 4000 - 0x4002 4FFF | Reserved |
| | | 0x4002 3C00 - 0x4002 3FFF | Reserved |
| | | 0x4002 3800 - 0x4002 3BFF | Reserved |
| | | 0x4002 3400 - 0x4002 37FF | Reserved |
| | | 0x4002 3000 - 0x4002 33FF | CRC |
| | | 0x4002 2C00 - 0x4002 2FFF | Reserved |
| | | 0x4002 2800 - 0x4002 2BFF | Reserved |
| | | 0x4002 2400 - 0x4002 27FF | Reserved |
| | | 0x4002 2000 - 0x4002 23FF | FMC |
| | | 0x4002 1C00 - 0x4002 1FFF | Reserved |
| | | 0x4002 1800 - 0x4002 1BFF | Reserved |
| | | 0x4002 1400 - 0x4002 17FF | Reserved |
| | | 0x4002 1000 - 0x4002 13FF | RCU |
| | | 0x4002 0C00 - 0x4002 0FFF | Reserved |
| | | 0x4002 0800 - 0x4002 0BFF | Reserved |
| | | 0x4002 0400 - 0x4002 07FF | DMA1 |
| | | 0x4002 0000 - 0x4002 03FF | DMA0 |
| | | 0x4001 8400 - 0x4001 FFFF | Reserved |
| | | 0x4001 8000 - 0x4001 83FF | Reserved |

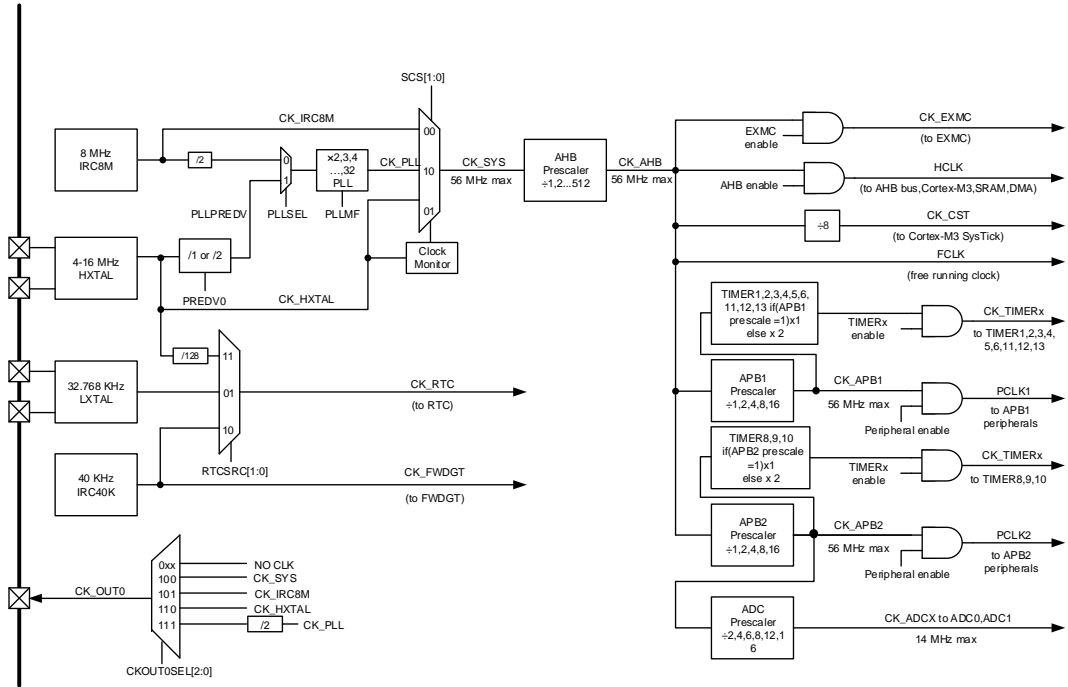
| Pre-defined Regions | Bus | Address | Peripherals |
|---------------------|---------------------------|---------------------------|-------------|
| | APB2 | 0x4001 7C00 - 0x4001 7FFF | Reserved |
| | | 0x4001 7800 - 0x4001 7BFF | Reserved |
| | | 0x4001 7400 - 0x4001 77FF | Reserved |
| | | 0x4001 7000 - 0x4001 73FF | Reserved |
| | | 0x4001 6C00 - 0x4001 6FFF | Reserved |
| | | 0x4001 6800 - 0x4001 6BFF | Reserved |
| | | 0x4001 5C00 - 0x4001 67FF | Reserved |
| | | 0x4001 5800 - 0x4001 5BFF | Reserved |
| | | 0x4001 5400 - 0x4001 57FF | TIMER10 |
| | | 0x4001 5000 - 0x4001 53FF | TIMER9 |
| | | 0x4001 4C00 - 0x4001 4FFF | TIMER8 |
| | | 0x4001 4800 - 0x4001 4BFF | Reserved |
| | | 0x4001 4400 - 0x4001 47FF | Reserved |
| | | 0x4001 4000 - 0x4001 43FF | Reserved |
| | | 0x4001 3C00 - 0x4001 3FFF | Reserved |
| | | 0x4001 3800 - 0x4001 3BFF | USART0 |
| | | 0x4001 3400 - 0x4001 37FF | Reserved |
| | | 0x4001 3000 - 0x4001 33FF | SPI0 |
| | | 0x4001 2C00 - 0x4001 2FFF | Reserved |
| | | 0x4001 2800 - 0x4001 2BFF | ADC1 |
| | | 0x4001 2400 - 0x4001 27FF | ADC0 |
| | | 0x4001 2000 - 0x4001 23FF | GPIOG |
| | | 0x4001 1C00 - 0x4001 1FFF | GPIOF |
| | | 0x4001 1800 - 0x4001 1BFF | GPIOE |
| | | 0x4001 1400 - 0x4001 17FF | GPIOD |
| | | 0x4001 1000 - 0x4001 13FF | GPIOC |
| | | 0x4001 0C00 - 0x4001 0FFF | GPIOB |
| | | 0x4001 0800 - 0x4001 0BFF | GPIOA |
| | 0x4001 0400 - 0x4001 07FF | EXTI | |
| | 0x4001 0000 - 0x4001 03FF | AFIO | |
| | APB1 | 0x4000 CC00 - 0x4000 FFFF | Reserved |
| | | 0x4000 C800 - 0x4000 CBFF | Reserved |
| | | 0x4000 C400 - 0x4000 C7FF | Reserved |
| | | 0x4000 C000 - 0x4000 C3FF | Reserved |
| | | 0x4000 8000 - 0x4000 BFFF | Reserved |
| | | 0x4000 7C00 - 0x4000 7FFF | Reserved |
| | | 0x4000 7800 - 0x4000 7BFF | Reserved |
| | | 0x4000 7400 - 0x4000 77FF | Reserved |
| | | 0x4000 7000 - 0x4000 73FF | PMU |
| | | 0x4000 6C00 - 0x4000 6FFF | BKP |

| Pre-defined Regions | Bus | Address | Peripherals |
|---------------------------|--------|---------------------------|--------------|
| | | 0x4000 6800 - 0x4000 6BFF | Reserved |
| | | 0x4000 6400 - 0x4000 67FF | Reserved |
| | | 0x4000 6000 - 0x4000 63FF | Reserved |
| | | 0x4000 5C00 - 0x4000 5FFF | Reserved |
| | | 0x4000 5800 - 0x4000 5BFF | I2C1 |
| | | 0x4000 5400 - 0x4000 57FF | I2C0 |
| | | 0x4000 5000 - 0x4000 53FF | UART4 |
| | | 0x4000 4C00 - 0x4000 4FFF | UART3 |
| | | 0x4000 4800 - 0x4000 4BFF | USART2 |
| | | 0x4000 4400 - 0x4000 47FF | USART1 |
| | | 0x4000 4000 - 0x4000 43FF | Reserved |
| | | 0x4000 3C00 - 0x4000 3FFF | SPI2 |
| | | 0x4000 3800 - 0x4000 3BFF | SPI1 |
| | | 0x4000 3400 - 0x4000 37FF | Reserved |
| | | 0x4000 3000 - 0x4000 33FF | FWDGT |
| | | 0x4000 2C00 - 0x4000 2FFF | WWDGT |
| | | 0x4000 2800 - 0x4000 2BFF | RTC |
| | | 0x4000 2400 - 0x4000 27FF | Reserved |
| | | 0x4000 2000 - 0x4000 23FF | TIMER13 |
| | | 0x4000 1C00 - 0x4000 1FFF | TIMER12 |
| | | 0x4000 1800 - 0x4000 1BFF | TIMER11 |
| | | 0x4000 1400 - 0x4000 17FF | TIMER6 |
| | | 0x4000 1000 - 0x4000 13FF | TIMER5 |
| | | 0x4000 0C00 - 0x4000 0FFF | TIMER4 |
| 0x4000 0800 - 0x4000 0BFF | TIMER3 | | |
| 0x4000 0400 - 0x4000 07FF | TIMER2 | | |
| 0x4000 0000 - 0x4000 03FF | TIMER1 | | |
| SRAM | AHB | 0x2007 0000 - 0x3FFF FFFF | Reserved |
| | | 0x2006 0000 - 0x2006 FFFF | Reserved |
| | | 0x2003 0000 - 0x2005 FFFF | Reserved |
| | | 0x2002 0000 - 0x2002 FFFF | Reserved |
| | | 0x2001 C000 - 0x2001 FFFF | Reserved |
| | | 0x2001 8000 - 0x2001 BFFF | Reserved |
| | | 0x2000 0000 - 0x2001 3FFF | SRAM |
| Code | AHB | 0x1FFF F810 - 0x1FFF FFFF | Reserved |
| | | 0x1FFF F800 - 0x1FFF F80F | Option Bytes |
| | | 0x1FFF B000 - 0x1FFF F7FF | Boot loader |
| | | 0x1FFF 7A10 - 0x1FFF AFFF | Reserved |
| | | 0x1FFF 7800 - 0x1FFF 7A0F | Reserved |
| | | 0x1FFF 0000 - 0x1FFF 77FF | Reserved |

| Pre-defined Regions | Bus | Address | Peripherals |
|---------------------|-----|---------------------------|--------------------------------------|
| | | 0x1FFE C010 - 0x1FFE FFFF | Reserved |
| | | 0x1FFE C000 - 0x1FFE C00F | Reserved |
| | | 0x1001 0000 - 0x1FFE BFFF | Reserved |
| | | 0x1000 0000 - 0x1000 FFFF | Reserved |
| | | 0x083C 0000 - 0x0FFF FFFF | Reserved |
| | | 0x0830 0000 - 0x083B FFFF | Reserved |
| | | 0x0800 0000 - 0x082F FFFF | Main Flash |
| | | 0x0030 0000 - 0x07FF FFFF | Reserved |
| | | 0x0000 0000 - 0x002F FFFF | Aliased to Main Flash or Boot loader |

2.5. Clock tree

Figure 2-8. GD32F101xx clock tree



Legend:

- HXTAL: High speed external clock
- LXTAL: Low speed external clock
- IRC8M: High speed internal clock
- IRC40K: Low speed internal clock

2.6. Pin definitions

2.6.1. GD32F101Zx LQFP144 pin definitions

Table 2-5. GD32F101Zx LQFP144 pin definitions

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|-------------------|------|-------------------------|--------------------------|----------------------------------------------------------------------------------|
| PE2 | 1 | I/O | 5VT | Default: PE2 Alternate: TRACECK, EXMC_A23 |
| PE3 | 2 | I/O | 5VT | Default: PE3 Alternate: TRACED0, EXMC_A19 |
| PE4 | 3 | I/O | 5VT | Default: PE4 Alternate: TRACED1, EXMC_A20 |
| PE5 | 4 | I/O | 5VT | Default: PE5 Alternate: TRACED2, EXMC_A21 Remap: TIMER8_CH0 ⁽³⁾ |
| PE6 | 5 | I/O | 5VT | Default: PE6 Alternate: TRACED3, EXMC_A22 Remap: TIMER8_CH1 ⁽³⁾ |
| V _{BAT} | 6 | P | | Default: V _{BAT} |
| PC13-TAMPER-RTC | 7 | I/O | | Default: PC13 Alternate: TAMPER-RTC |
| PC14-OSC32IN | 8 | I/O | | Default: PC14 Alternate: OSC32IN |
| PC15-OSC32OUT | 9 | I/O | | Default: PC15 Alternate: OSC32OUT |
| PF0 | 10 | I/O | 5VT | Default: PF0 Alternate: EXMC_A0 |
| PF1 | 11 | I/O | 5VT | Default: PF1 Alternate: EXMC_A1 |
| PF2 | 12 | I/O | 5VT | Default: PF2 Alternate: EXMC_A2 |
| PF3 | 13 | I/O | 5VT | Default: PF3 Alternate: EXMC_A3 |
| PF4 | 14 | I/O | 5VT | Default: PF4 Alternate: EXMC_A4 |
| PF5 | 15 | I/O | 5VT | Default: PF5 Alternate: EXMC_A5 |
| V _{SS_5} | 16 | P | | Default: V _{SS_5} |
| V _{DD_5} | 17 | P | | Default: V _{DD_5} |
| PF6 | 18 | I/O | | Default: PF6 Alternate: EXMC_NIORD |

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|-------------------|------|-------------------------|--------------------------|-----------------------------------------------------------------------------------------------------------------------|
| | | | | Remap: TIMER9_CH0 ⁽³⁾ |
| PF7 | 19 | I/O | | Default: PF7 Alternate: EXMC_NREG Remap: TIMER10_CH0 ⁽³⁾ |
| PF8 | 20 | I/O | | Default: PF8 Alternate: EXMC_NIOWR Remap: TIMER12_CH0 ⁽³⁾ |
| PF9 | 21 | I/O | | Default: PF9 Alternate: EXMC_CD Remap: TIMER13_CH0 ⁽³⁾ |
| PF10 | 22 | I/O | | Default: PF10 Alternate: EXMC_INTR |
| OSCIN | 23 | I | | Default: OSCIN Remap: PD0 |
| OSCOUT | 24 | O | | Default: OSCOUT Remap: PD1 |
| NRST | 25 | I/O | | Default: NRST |
| PC0 | 26 | I/O | | Default: PC0 Alternate: ADC01_IN10 ⁽⁴⁾ |
| PC1 | 27 | I/O | | Default: PC1 Alternate: ADC01_IN11 ⁽⁴⁾ |
| PC2 | 28 | I/O | | Default: PC2 Alternate: ADC01_IN12 ⁽⁴⁾ |
| PC3 | 29 | I/O | | Default: PC3 Alternate: ADC01_IN13 ⁽⁴⁾ |
| V _{SSA} | 30 | P | | Default: V _{SSA} |
| V _{REF-} | 31 | P | | Default: V _{REF-} |
| V _{REF+} | 32 | P | | Default: V _{REF+} |
| V _{DDA} | 33 | P | | Default: V _{DDA} |
| PA0-WKUP | 34 | I/O | | Default: PA0 Alternate: WKUP, USART1_CTS, ADC01_IN0 ⁽⁴⁾ , TIMER1_CH0, TIMER1_ETI, TIMER4_CH0 |
| PA1 | 35 | I/O | | Default: PA1 Alternate: USART1_RTS, ADC01_IN1 ⁽⁴⁾ , TIMER1_CH1, TIMER4_CH1 |
| PA2 | 36 | I/O | | Default: PA2 Alternate: USART1_TX, ADC01_IN2 ⁽⁴⁾ , TIMER1_CH2, TIMER4_CH2, TIMER8_CH0 ⁽³⁾ |
| PA3 | 37 | I/O | | Default: PA3 Alternate: USART1_RX, ADC01_IN3 ⁽⁴⁾ , TIMER1_CH3, TIMER4_CH3, TIMER8_CH1 ⁽³⁾ |
| V _{SS_4} | 38 | P | | Default: V _{SS_4} |

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|-------------------|------|-------------------------|--------------------------|------------------------------------------------------------------------------------------------------------|
| V _{DD_4} | 39 | P | | Default: V _{DD_4} |
| PA4 | 40 | I/O | | Default: PA4 Alternate: SPI0_NSS, USART1_CK, ADC01_IN4 ⁽⁴⁾ Remap:SPI2_NSS |
| PA5 | 41 | I/O | | Default: PA5 Alternate: SPI0_SCK, ADC01_IN5 ⁽⁴⁾ |
| PA6 | 42 | I/O | | Default: PA6 Alternate: SPI0_MISO, ADC01_IN6 ⁽⁴⁾ , TIMER2_CH0, TIMER12_CH0 ⁽³⁾ |
| PA7 | 43 | I/O | | Default: PA7 Alternate: SPI0_MOSI, ADC01_IN7 ⁽⁴⁾ , TIMER2_CH1, TIMER13_CH0 ⁽³⁾ |
| PC4 | 44 | I/O | | Default: PC4 Alternate: ADC01_IN14 ⁽⁴⁾ |
| PC5 | 45 | I/O | | Default: PC5 Alternate: ADC01_IN15 ⁽⁴⁾ |
| PB0 | 46 | I/O | | Default: PB0 Alternate: ADC01_IN8 ⁽⁴⁾ , TIMER2_CH2 |
| PB1 | 47 | I/O | | Default: PB1 Alternate: ADC01_IN9 ⁽⁴⁾ , TIMER2_CH3 |
| PB2 | 48 | I/O | 5VT | Default: PB2/BOOT1 |
| PF11 | 49 | I/O | 5VT | Default: PF11 Alternate: EXMC_NIOS16 |
| PF12 | 50 | I/O | 5VT | Default: PF12 Alternate: EXMC_A6 |
| V _{SS_6} | 51 | P | | Default: V _{SS_6} |
| V _{DD_6} | 52 | P | | Default: V _{DD_6} |
| PF13 | 53 | I/O | 5VT | Default: PF13 Alternate: EXMC_A7 |
| PF14 | 54 | I/O | 5VT | Default: PF14 Alternate: EXMC_A8 |
| PF15 | 55 | I/O | 5VT | Default: PF15 Alternate: EXMC_A9 |
| PG0 | 56 | I/O | 5VT | Default: PG0 Alternate: EXMC_A10 |
| PG1 | 57 | I/O | 5VT | Default: PG1 Alternate: EXMC_A11 |
| PE7 | 58 | I/O | 5VT | Default: PE7 Alternate: EXMC_D4 |
| PE8 | 59 | I/O | 5VT | Default: PE8 Alternate: EXMC_D5 |
| PE9 | 60 | I/O | 5VT | Default: PE9 Alternate: EXMC_D6 |

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|-------------------|------|-------------------------|--------------------------|-------------------------------------------------------------------------------|
| V _{SS_7} | 61 | P | | Default: V _{SS_7} |
| V _{DD_7} | 62 | P | | Default: V _{DD_7} |
| PE10 | 63 | I/O | 5VT | Default: PE10 Alternate: EXMC_D7 |
| PE11 | 64 | I/O | 5VT | Default: PE11 Alternate: EXMC_D8 |
| PE12 | 65 | I/O | 5VT | Default: PE12 Alternate: EXMC_D9 |
| PE13 | 66 | I/O | 5VT | Default: PE13 Alternate: EXMC_D10 |
| PE14 | 67 | I/O | 5VT | Default: PE14 Alternate: EXMC_D11 |
| PE15 | 68 | I/O | 5VT | Default: PE15 Alternate: EXMC_D12 |
| PB10 | 69 | I/O | 5VT | Default: PB10 Alternate: I2C1_SCL, USART2_TX Remap: TIMER1_CH2 |
| PB11 | 70 | I/O | 5VT | Default: PB11 Alternate: I2C1_SDA, USART2_RX Remap: TIMER1_CH3 |
| V _{SS_1} | 71 | P | | Default: V _{SS_1} |
| V _{DD_1} | 72 | P | | Default: V _{DD_1} |
| PB12 | 73 | I/O | 5VT | Default: PB12 Alternate: SPI1_NSS, I2C1_SMBA, USART2_CK |
| PB13 | 74 | I/O | 5VT | Default: PB13 Alternate: SPI1_SCK, USART2_CTS |
| PB14 | 75 | I/O | 5VT | Default: PB14 Alternate: SPI1_MISO, USART2_RTS, TIMER11_CH0 ⁽³⁾ |
| PB15 | 76 | I/O | 5VT | Default: PB15 Alternate: SPI1_MOSI, TIMER11_CH1 ⁽³⁾ |
| PD8 | 77 | I/O | 5VT | Default: PD8 Alternate: EXMC_D13 Remap: USART2_TX |
| PD9 | 78 | I/O | 5VT | Default: PD9 Alternate: EXMC_D14 Remap: USART2_RX |
| PD10 | 79 | I/O | 5VT | Default: PD10 Alternate: EXMC_D15 Remap: USART2_CK |
| PD11 | 80 | I/O | 5VT | Default: PD11 Alternate: EXMC_A16 Remap: USART2_CTS |
| PD12 | 81 | I/O | 5VT | Default: PD12 |

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|-------------------|------|-------------------------|--------------------------|-----------------------------------------------------------|
| | | | | Alternate: EXMC_A17 Remap: TIMER3_CH0, USART2_RTS |
| PD13 | 82 | I/O | 5VT | Default: PD13 Alternate: EXMC_A18 Remap: TIMER3_CH1 |
| V _{SS_8} | 83 | P | | Default: V _{SS_8} |
| V _{DD_8} | 84 | P | | Default: V _{DD_8} |
| PD14 | 85 | I/O | 5VT | Default: PD14 Alternate: EXMC_D0 Remap: TIMER3_CH2 |
| PD15 | 86 | I/O | 5VT | Default: PD15 Alternate: EXMC_D1 Remap: TIMER3_CH3 |
| PG2 | 87 | I/O | 5VT | Default: PG2 Alternate: EXMC_A12 |
| PG3 | 88 | I/O | 5VT | Default: PG3 Alternate: EXMC_A13 |
| PG4 | 89 | I/O | 5VT | Default: PG4 Alternate: EXMC_A14 |
| PG5 | 90 | I/O | 5VT | Default: PG5 Alternate: EXMC_A15 |
| PG6 | 91 | I/O | 5VT | Default: PG6 Alternate: EXMC_INT1 |
| PG7 | 92 | I/O | 5VT | Default: PG7 Alternate: EXMC_INT2 |
| PG8 | 93 | I/O | 5VT | Default: PG8 |
| V _{SS_9} | 94 | P | | Default: V _{SS_9} |
| V _{DD_9} | 95 | P | | Default: V _{DD_9} |
| PC6 | 96 | I/O | 5VT | Default: PC6 Remap: TIMER2_CH0 |
| PC7 | 97 | I/O | 5VT | Default: PC7 Remap: TIMER2_CH1 |
| PC8 | 98 | I/O | 5VT | Default: PC8 Remap: TIMER2_CH2 |
| PC9 | 99 | I/O | 5VT | Default: PC9 Remap: TIMER2_CH3 |
| PA8 | 100 | I/O | 5VT | Default: PA8 Alternate: USART0_CK, CK_OUT0 |
| PA9 | 101 | I/O | 5VT | Default: PA9 Alternate: USART0_TX |
| PA10 | 102 | I/O | 5VT | Default: PA10 Alternate: USART0_RX |

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|--------------------|------|-------------------------|--------------------------|---------------------------------------------------------------------------------------|
| PA11 | 103 | I/O | 5VT | Default: PA11 Alternate: USART0_CTS |
| PA12 | 104 | I/O | 5VT | Default: PA12 Alternate: USART0_RTS |
| PA13 | 105 | I/O | 5VT | Default: JTMS, SWDIO Remap: PA13 |
| NC | 106 | | | - |
| V _{SS_2} | 107 | P | | Default: V _{SS_2} |
| V _{DD_2} | 108 | P | | Default: V _{DD_2} |
| PA14 | 109 | I/O | 5VT | Default: JTCK, SWCLK Remap: PA14 |
| PA15 | 110 | I/O | 5VT | Default: JTDI Alternate: SPI2_NSS Remap: TIMER1_CH0, TIMER1_ETI, PA15, SPI0_NSS |
| PC10 | 111 | I/O | 5VT | Default: PC10 Alternate: UART3_TX Remap: USART2_TX, SPI2_SCK |
| PC11 | 112 | I/O | 5VT | Default: PC11 Alternate: UART3_RX Remap: USART2_RX, SPI2_MISO |
| PC12 | 113 | I/O | 5VT | Default: PC12 Alternate: UART4_TX Remap: USART2_CK, SPI2_MOSI |
| PD0 | 114 | I/O | 5VT | Default: PD0 Alternate: EXMC_D2 Remap: OSCIN |
| PD1 | 115 | I/O | 5VT | Default: PD1 Alternate: EXMC_D3 Remap: OSCOUT |
| PD2 | 116 | I/O | 5VT | Default: PD2 Alternate: TIMER2_ETI, UART4_RX |
| PD3 | 117 | I/O | 5VT | Default: PD3 Alternate: EXMC_CLK Remap: USART1_CTS |
| PD4 | 118 | I/O | 5VT | Default: PD4 Alternate: EXMC_NOE Remap: USART1_RTS |
| PD5 | 119 | I/O | 5VT | Default: PD5 Alternate: EXMC_NWE Remap: USART1_TX |
| V _{SS_10} | 120 | | | Default: V _{SS_10} |
| V _{DD_10} | 121 | | | Default: V _{DD_10} |
| PD6 | 122 | I/O | 5VT | Default: PD6 |

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|--------------------|------|-------------------------|--------------------------|--------------------------------------------------------------------------------------|
| | | | | Alternate: EXMC_NWAIT Remap: USART1_RX |
| PD7 | 123 | I/O | 5VT | Default: PD7 Alternate: EXMC_NE0, EXMC_NCE1 Remap: USART1_CK |
| PG9 | 124 | I/O | 5VT | Default: PG9 Alternate: EXMC_NE1, EXMC_NCE2 |
| PG10 | 125 | I/O | 5VT | Default: PG10 Alternate: EXMC_NCE3_0, EXMC_NE2 |
| PG11 | 126 | I/O | 5VT | Default: PG11 Alternate: EXMC_NCE3_1 |
| PG12 | 127 | I/O | 5VT | Default: PG12 Alternate: EXMC_NE3 |
| PG13 | 128 | I/O | 5VT | Default: PG13 Alternate: EXMC_A24 |
| PG14 | 129 | I/O | 5VT | Default: PG14 Alternate: EXMC_A25 |
| V _{SS_11} | 130 | P | | Default: V _{SS_10} |
| V _{DD_11} | 131 | P | | Default: V _{DD_10} |
| PG15 | 132 | I/O | 5VT | Default: PG15 |
| PB3 | 133 | I/O | 5VT | Default: JTDO Alternate: SPI2_SCK Remap: PB3, TRACESWO, TIMER1_CH1, SPI0_SCK |
| PB4 | 134 | I/O | 5VT | Default: NJTRST Alternate: SPI2_MISO Remap: TIMER2_CH0, PB4, SPI0_MISO |
| PB5 | 135 | I/O | | Default: PB5 Alternate: I2C0_SMBA, SPI2_MOSI Remap: TIMER2_CH1, SPI0_MOSI |
| PB6 | 136 | I/O | 5VT | Default: PB6 Alternate: I2C0_SCL, TIMER3_CH0 Remap: USART0_TX |
| PB7 | 137 | I/O | 5VT | Default: PB7 Alternate: I2C0_SDA, TIMER3_CH1, EXMC_NADV Remap: USART0_RX |
| BOOT0 | 138 | I | | Default: BOOT0 |
| PB8 | 139 | I/O | 5VT | Default: PB8 Alternate: TIMER3_CH2, TIMER9_CH0 ⁽³⁾ Remap: I2C0_SCL |
| PB9 | 140 | I/O | 5VT | Default: PB9 Alternate: TIMER3_CH3, TIMER10_CH0 ⁽³⁾ Remap: I2C0_SDA |
| PE0 | 141 | I/O | 5VT | Default: PE0 |

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|-------------------|------|-------------------------|--------------------------|--------------------------------------|
| | | | | Alternate: TIMER3_ETI, EXMC_NBL0 |
| PE1 | 142 | I/O | 5VT | Default: PE1 Alternate: EXMC_NBL1 |
| V _{SS_3} | 143 | P | | Default: V _{SS_3} |
| V _{DD_3} | 144 | P | | Default: V _{DD_3} |

Notes:

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) Functions are available in GD32F101ZF/G//K devices.

(4) In GD32F101ZF/G//K devices, functions are fully available for ADC0 and ADC1; In GD32F101ZC/D/E devices, functions are available for ADC0.

2.6.2. GD32F101Vx LQFP100 pin definitions
Table 2-6. GD32F101Vx LQFP100 pin definitions

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|-------------------|------|-------------------------|--------------------------|----------------------------------------------------------------------------------|
| PE2 | 1 | I/O | 5VT | Default: PE2 Alternate: TRACECK, EXMC_A23 |
| PE3 | 2 | I/O | 5VT | Default: PE3 Alternate: TRACED0, EXMC_A19 |
| PE4 | 3 | I/O | 5VT | Default: PE4 Alternate: TRACED1, EXMC_A20 |
| PE5 | 4 | I/O | 5VT | Default: PE5 Alternate: TRACED2, EXMC_A21 Remap: TIMER8_CH0 ⁽⁴⁾ |
| PE6 | 5 | I/O | 5VT | Default: PE6 Alternate: TRACED3, EXMC_A22 Remap: TIMER8_CH1 ⁽⁴⁾ |
| V _{BAT} | 6 | P | | Default: V _{BAT} |
| PC13-TAMPER-RTC | 7 | I/O | | Default: PC13 Alternate: TAMPER-RTC |
| PC14-OSC32IN | 8 | I/O | | Default: PC14 Alternate: OSC32IN |
| PC15-OSC32OUT | 9 | I/O | | Default: PC15 Alternate: OSC32OUT |
| V _{SS_5} | 10 | P | | Default: V _{SS_5} |
| V _{DD_5} | 11 | P | | Default: V _{DD_5} |
| OSCIN | 12 | I | | Default: OSCIN Remap: PD0 |
| OSCOUT | 13 | O | | Default: OSCOUT Remap: PD1 |
| NRST | 14 | I/O | | Default: NRST |
| PC0 | 15 | I/O | | Default: PC0 Alternate: ADC01_IN10 ⁽⁵⁾ |
| PC1 | 16 | I/O | | Default: PC1 Alternate: ADC01_IN11 ⁽⁵⁾ |
| PC2 | 17 | I/O | | Default: PC2 Alternate: ADC01_IN12 ⁽⁵⁾ |
| PC3 | 18 | I/O | | Default: PC3 Alternate: ADC01_IN13 ⁽⁵⁾ |
| V _{SSA} | 19 | P | | Default: V _{SSA} |
| V _{REF-} | 20 | P | | Default: V _{REF-} |
| V _{REF+} | 21 | P | | Default: V _{REF+} |

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|-------------------|------|-------------------------|--------------------------|---------------------------------------------------------------------------------------------------------------------------------------|
| V _{DDA} | 22 | P | | Default: V _{DDA} |
| PA0-WKUP | 23 | I/O | | Default: PA0 Alternate: WKUP, USART1_CTS, ADC01_IN0 ⁽⁵⁾ , TIMER1_CH0, TIMER1_ETI, TIMER4_CH0 ⁽³⁾ |
| PA1 | 24 | I/O | | Default: PA1 Alternate: USART1_RTS, ADC01_IN1 ⁽⁵⁾ , TIMER1_CH1, TIMER4_CH1 ⁽³⁾ |
| PA2 | 25 | I/O | | Default: PA2 Alternate: USART1_TX, ADC01_IN2 ⁽⁵⁾ , TIMER1_CH2, TIMER4_CH2 ⁽³⁾ , TIMER8_CH0 ⁽⁴⁾ |
| PA3 | 26 | I/O | | Default: PA3 Alternate: USART1_RX, ADC01_IN3 ⁽⁵⁾ , TIMER1_CH3, TIMER4_CH3 ⁽³⁾ , TIMER8_CH1 ⁽⁴⁾ |
| V _{SS_4} | 27 | P | | Default: V _{SS_4} |
| V _{DD_4} | 28 | P | | Default: V _{DD_4} |
| PA4 | 29 | I/O | | Default: PA4 Alternate: SPI0_NSS, USART1_CK, ADC01_IN4 ⁽⁵⁾ Remap:SPI2_NSS ⁽³⁾ |
| PA5 | 30 | I/O | | Default: PA5 Alternate: SPI0_SCK, ADC01_IN5 ⁽⁵⁾ |
| PA6 | 31 | I/O | | Default: PA6 Alternate: SPI0_MISO, ADC01_IN6 ⁽⁵⁾ , TIMER2_CH0, TIMER12_CH0 ⁽⁴⁾ |
| PA7 | 32 | I/O | | Default: PA7 Alternate: SPI0_MOSI, ADC01_IN7 ⁽⁵⁾ , TIMER2_CH1, TIMER13_CH0 ⁽⁴⁾ |
| PC4 | 33 | I/O | | Default: PC4 Alternate: ADC01_IN14 ⁽⁵⁾ |
| PC5 | 34 | I/O | | Default: PC5 Alternate: ADC01_IN15 ⁽⁵⁾ |
| PB0 | 35 | I/O | | Default: PB0 Alternate: ADC01_IN8 ⁽⁵⁾ , TIMER2_CH2 |
| PB1 | 36 | I/O | | Default: PB1 Alternate: ADC01_IN9 ⁽⁵⁾ , TIMER2_CH3 |
| PB2 | 37 | I/O | 5VT | Default: PB2/BOOT1 |
| PE7 | 38 | I/O | 5VT | Default: PE7 Alternate: EXMC_D4 |
| PE8 | 39 | I/O | 5VT | Default: PE8 Alternate: EXMC_D5 |
| PE9 | 40 | I/O | 5VT | Default: PE9 Alternate: EXMC_D6 |
| PE10 | 41 | I/O | 5VT | Default: PE10 |

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|-------------------|------|-------------------------|--------------------------|-------------------------------------------------------------------------------|
| | | | | Alternate: EXMC_D7 |
| PE11 | 42 | I/O | 5VT | Default: PE11 Alternate: EXMC_D8 |
| PE12 | 43 | I/O | 5VT | Default: PE12 Alternate: EXMC_D9 |
| PE13 | 44 | I/O | 5VT | Default: PE13 Alternate: EXMC_D10 |
| PE14 | 45 | I/O | 5VT | Default: PE14 Alternate: EXMC_D11 |
| PE15 | 46 | I/O | 5VT | Default: PE15 Alternate: EXMC_D12 |
| PB10 | 47 | I/O | 5VT | Default: PB10 Alternate: I2C1_SCL, USART2_TX Remap: TIMER1_CH2 |
| PB11 | 48 | I/O | 5VT | Default: PB11 Alternate: I2C1_SDA, USART2_RX Remap: TIMER1_CH3 |
| V _{SS_1} | 49 | P | | Default: V _{SS_1} |
| V _{DD_1} | 50 | P | | Default: V _{DD_1} |
| PB12 | 51 | I/O | 5VT | Default: PB12 Alternate: SPI1_NSS, I2C1_SMBA, USART2_CK |
| PB13 | 52 | I/O | 5VT | Default: PB13 Alternate: SPI1_SCK, USART2_CTS |
| PB14 | 53 | I/O | 5VT | Default: PB14 Alternate: SPI1_MISO, USART2_RTS, TIMER11_CH0 ⁽⁴⁾ |
| PB15 | 54 | I/O | 5VT | Default: PB15 Alternate: SPI1_MOSI, TIMER11_CH1 ⁽⁴⁾ |
| PD8 | 55 | I/O | 5VT | Default: PD8 Alternate: EXMC_D13 Remap: USART2_TX |
| PD9 | 56 | I/O | 5VT | Default: PD9 Alternate: EXMC_D14 Remap: USART2_RX |
| PD10 | 57 | I/O | 5VT | Default: PD10 Alternate: EXMC_D15 Remap: USART2_CK |
| PD11 | 58 | I/O | 5VT | Default: PD11 Alternate: EXMC_A16 Remap: USART2_CTS |
| PD12 | 59 | I/O | 5VT | Default: PD12 Alternate: EXMC_A17 Remap: TIMER3_CH0, USART2_RTS |

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|-------------------|------|-------------------------|--------------------------|------------------------------------------------------------------------------------------------------|
| PD13 | 60 | I/O | 5VT | Default: PD13 Alternate: EXMC_A18 Remap: TIMER3_CH1 |
| PD14 | 61 | I/O | 5VT | Default: PD14 Alternate: EXMC_D0 Remap: TIMER3_CH2 |
| PD15 | 62 | I/O | 5VT | Default: PD15 Alternate: EXMC_D1 Remap: TIMER3_CH3 |
| PC6 | 63 | I/O | 5VT | Default: PC6 Remap: TIMER2_CH0 |
| PC7 | 64 | I/O | 5VT | Default: PC7 Remap: TIMER2_CH1 |
| PC8 | 65 | I/O | 5VT | Default: PC8 Remap: TIMER2_CH2 |
| PC9 | 66 | I/O | 5VT | Default: PC9 Remap: TIMER2_CH3 |
| PA8 | 67 | I/O | 5VT | Default: PA8 Alternate: USART0_CK, CK_OUT0 |
| PA9 | 68 | I/O | 5VT | Default: PA9 Alternate: USART0_TX |
| PA10 | 69 | I/O | 5VT | Default: PA10 Alternate: USART0_RX |
| PA11 | 70 | I/O | 5VT | Default: PA11 Alternate: USART0_CTS |
| PA12 | 71 | I/O | 5VT | Default: PA12 Alternate: USART0_RTS |
| PA13 | 72 | I/O | 5VT | Default: JTMS, SWDIO Remap: PA13 |
| NC | 73 | | | - |
| V _{SS_2} | 74 | P | | Default: V _{SS_2} |
| V _{DD_2} | 75 | P | | Default: V _{DD_2} |
| PA14 | 76 | I/O | 5VT | Default: JTCK, SWCLK Remap: PA14 |
| PA15 | 77 | I/O | 5VT | Default: JTDI Alternate: SPI2_NSS ⁽³⁾ Remap: TIMER1_CH0, TIMER1_ETI, PA15, SPI0_NSS |
| PC10 | 78 | I/O | 5VT | Default: PC10 Alternate: UART3_TX ⁽³⁾ Remap: USART2_TX, SPI2_SCK ⁽³⁾ |
| PC11 | 79 | I/O | 5VT | Default: PC11 Alternate: UART3_RX ⁽³⁾ , SPI2_MISO ⁽³⁾ |

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|----------|------|-------------------------|--------------------------|---------------------------------------------------------------------------------------------------|
| | | | | Remap: USART2_RX |
| PC12 | 80 | I/O | 5VT | Default: PC12 Alternate: UART4_TX ⁽³⁾ Remap: USART2_CK, SPI2_MOSI ⁽³⁾ |
| PD0 | 81 | I/O | 5VT | Default: PD0 Alternate: EXMC_D2 Remap: OSCIN |
| PD1 | 82 | I/O | 5VT | Default: PD1 Alternate: EXMC_D3 Remap: OSCOUT |
| PD2 | 83 | I/O | 5VT | Default: PD2 Alternate: TIMER2_ETI, UART4_RX ⁽³⁾ |
| PD3 | 84 | I/O | 5VT | Default: PD3 Alternate: EXMC_CLK Remap: USART1_CTS |
| PD4 | 85 | I/O | 5VT | Default: PD4 Alternate: EXMC_NOE Remap: USART1_RTS |
| PD5 | 86 | I/O | 5VT | Default: PD5 Alternate: EXMC_NWE Remap: USART1_TX |
| PD6 | 87 | I/O | 5VT | Default: PD6 Alternate: EXMC_NWAIT Remap: USART1_RX |
| PD7 | 88 | I/O | 5VT | Default: PD7 Alternate: EXMC_NE0/EXMC_NCE1 Remap: USART1_CK |
| PB3 | 89 | I/O | 5VT | Default: JTDO Alternate: SPI2_SCK ⁽³⁾ Remap: PB3, TRACESWO, TIMER1_CH1, SPI0_SCK |
| PB4 | 90 | I/O | 5VT | Default: NJTRST Alternate: SPI2_MISO ⁽³⁾ Remap: TIMER2_CH0, PB4, SPI0_MISO |
| PB5 | 91 | I/O | | Default: PB5 Alternate: I2C0_SMBA, SPI2_MOSI ⁽³⁾ Remap: TIMER2_CH1, SPI0_MOSI |
| PB6 | 92 | I/O | 5VT | Default: PB6 Alternate: I2C0_SCL, TIMER3_CH0, Remap: USART0_TX |
| PB7 | 93 | I/O | 5VT | Default: PB7 Alternate: I2C0_SDA, TIMER3_CH1, EXMC_NADV Remap: USART0_RX |

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|-------------------|------|-------------------------|--------------------------|--------------------------------------------------------------------------------------|
| BOOT0 | 94 | I | | Default: BOOT0 |
| PB8 | 95 | I/O | 5VT | Default: PB8 Alternate: TIMER3_CH2, TIMER9_CH0 ⁽⁴⁾ Remap: I2C0_SCL |
| PB9 | 96 | I/O | 5VT | Default: PB9 Alternate: TIMER3_CH3, TIMER10_CH0 ⁽⁴⁾ Remap: I2C0_SDA |
| PE0 | 97 | I/O | 5VT | Default: PE0 Alternate: TIMER3_ETI, EXMC_NBL0 |
| PE1 | 98 | I/O | 5VT | Default: PE1 Alternate: EXMC_NBL1 |
| V _{SS_3} | 99 | P | | Default: V _{SS_3} |
| V _{DD_3} | 100 | P | | Default: V _{DD_3} |

Notes:

(1) Type: I = input, O = output, P = power.

(2) I/O Level: 5VT = 5 V tolerant.

(3) Functions are available in GD32F101VC/D/E/F/G//K devices.

(4) Functions are available in GD32F101VF/G//K devices.

(5) In GD32F101VF/G//K devices, functions are fully available for ADC0 and ADC1; In GD32F101V8/B/C/D/E devices, functions are available for ADC0.

2.6.3. GD32F101Rx LQFP64 pin definitions
Table 2-7. GD32F101Rx LQFP64 pin definitions

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|-------------------|------|-------------------------|--------------------------|---------------------------------------------------------------------------------------------------------------------------------------|
| V _{BAT} | 1 | P | | Default: V _{BAT} |
| PC13-TAMPER-RTC | 2 | I/O | | Default: PC13 Alternate: TAMPER-RTC |
| PC14-OSC32IN | 3 | I/O | | Default: PC14 Alternate: OSC32IN |
| PC15-OSC32OUT | 4 | I/O | | Default: PC15 Alternate: OSC32OUT |
| OSCIN | 5 | I | | Default: OSCIN Remap: PD0 |
| OSCOUT | 6 | O | | Default: OSCOUT Remap: PD1 |
| NRST | 7 | I/O | | Default: NRST |
| PC0 | 8 | I/O | | Default: PC0 Alternate: ADC01_IN10 ⁽⁵⁾ |
| PC1 | 9 | I/O | | Default: PC1 Alternate: ADC01_IN11 ⁽⁵⁾ |
| PC2 | 10 | I/O | | Default: PC2 Alternate: ADC01_IN12 ⁽⁵⁾ |
| PC3 | 11 | I/O | | Default: PC3 Alternate: ADC01_IN13 ⁽⁵⁾ |
| V _{SSA} | 12 | P | | Default: V _{SSA} |
| V _{DDA} | 13 | P | | Default: V _{DDA} |
| PA0-WKUP | 14 | I/O | | Default: PA0 Alternate: WKUP, USART1_CTS, ADC01_IN0 ⁽⁵⁾ , TIMER1_CH0, TIMER1_ETI, TIMER4_CH0 ⁽³⁾ |
| PA1 | 15 | I/O | | Default: PA1 Alternate: USART1_RTS, ADC01_IN1 ⁽⁵⁾ , TIMER1_CH1, TIMER4_CH1 ⁽³⁾ |
| PA2 | 16 | I/O | | Default: PA2 Alternate: USART1_TX, ADC01_IN2 ⁽⁵⁾ , TIMER1_CH2, TIMER4_CH2 ⁽³⁾ , TIMER8_CH0 ⁽⁴⁾ |
| PA3 | 17 | I/O | | Default: PA3 Alternate: USART1_RX, ADC01_IN3 ⁽⁵⁾ , TIMER1_CH3, TIMER4_CH3 ⁽³⁾ , TIMER8_CH1 ⁽⁴⁾ |
| V _{SS_4} | 18 | P | | Default: V _{SS_4} |
| V _{DD_4} | 19 | P | | Default: V _{DD_4} |
| PA4 | 20 | I/O | | Default: PA4 Alternate: SPI0_NSS, USART1_CK, ADC01_IN4 ⁽⁵⁾ |

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|-------------------|------|-------------------------|--------------------------|---------------------------------------------------------------------------------------------------------------|
| | | | | Remap:SPI2_NSS ⁽³⁾ |
| PA5 | 21 | I/O | | Default: PA5 Alternate: SPI0_SCK, ADC01_IN5 ⁽⁵⁾ |
| PA6 | 22 | I/O | | Default: PA6 Alternate: SPI0_MISO, ADC01_IN6 ⁽⁵⁾ , TIMER2_CH0, TIMER12_CH0 ⁽⁴⁾ |
| PA7 | 23 | I/O | | Default: PA7 Alternate: SPI0_MOSI, ADC01_IN7 ⁽⁵⁾ , TIMER2_CH1, TIMER13_CH0 ⁽⁴⁾ |
| PC4 | 24 | I/O | | Default: PC4 Alternate: ADC01_IN14 ⁽⁵⁾ |
| PC5 | 25 | I/O | | Default: PC5 Alternate: ADC01_IN15 ⁽⁵⁾ |
| PB0 | 26 | I/O | | Default: PB0 Alternate: ADC01_IN8 ⁽⁵⁾ , TIMER2_CH2 |
| PB1 | 27 | I/O | | Default: PB1 Alternate: ADC01_IN9 ⁽⁵⁾ , TIMER2_CH3 |
| PB2 | 28 | I/O | 5VT | Default: PB2/BOOT1 |
| PB10 | 29 | I/O | 5VT | Default: PB10 Alternate: I2C1_SCL ⁽⁶⁾ , USART2_TX ⁽⁶⁾ Remap: TIMER1_CH2 |
| PB11 | 30 | I/O | 5VT | Default: PB11 Alternate: I2C1_SDA ⁽⁶⁾ , USART2_RX ⁽⁶⁾ Remap: TIMER1_CH3 |
| V _{SS_1} | 31 | P | | Default: V _{SS_1} |
| V _{DD_1} | 32 | P | | Default: V _{DD_1} |
| PB12 | 33 | I/O | 5VT | Default: PB12 Alternate: SPI1_NSS ⁽⁶⁾ , I2C1_SMBA ⁽⁶⁾ , USART2_CK ⁽⁶⁾ |
| PB13 | 34 | I/O | 5VT | Default: PB13 Alternate: SPI1_SCK ⁽⁶⁾ , USART2_CTS ⁽⁶⁾ |
| PB14 | 35 | I/O | 5VT | Default: PB14 Alternate: SPI1_MISO ⁽⁶⁾ , USART2_RTS ⁽⁶⁾ , TIMER11_CH0 ⁽⁴⁾ |
| PB15 | 36 | I/O | 5VT | Default: PB15 Alternate: SPI1_MOSI ⁽⁶⁾ , TIMER11_CH1 ⁽⁴⁾ |
| PC6 | 37 | I/O | 5VT | Default: PC6 Remap: TIMER2_CH0 |
| PC7 | 38 | I/O | 5VT | Default: PC7 Remap: TIMER2_CH1 |
| PC8 | 39 | I/O | 5VT | Default: PC8 Remap: TIMER2_CH2 |
| PC9 | 40 | I/O | 5VT | Default: PC9 Remap: TIMER2_CH3 |

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|-------------------|------|-------------------------|--------------------------|-------------------------------------------------------------------------------------------------------------------|
| PA8 | 41 | I/O | 5VT | Default: PA8 Alternate: USART0_CK, CK_OUT0 |
| PA9 | 42 | I/O | 5VT | Default: PA9 Alternate: USART0_TX |
| PA10 | 43 | I/O | 5VT | Default: PA10 Alternate: USART0_RX |
| PA11 | 44 | I/O | 5VT | Default: PA11 Alternate: USART0_CTS |
| PA12 | 45 | I/O | 5VT | Default: PA12 Alternate: USART0_RTS |
| PA13 | 46 | I/O | 5VT | Default: JTMS, SWDIO Remap: PA13 |
| NC | - | | | - |
| V _{SS_2} | 47 | P | | Default: V _{SS_2} |
| V _{DD_2} | 48 | P | | Default: V _{DD_2} |
| PA14 | 49 | I/O | 5VT | Default: JTCK, SWCLK Remap: PA14 |
| PA15 | 50 | I/O | 5VT | Default: JTDI Alternate: SPI2_NSS ⁽³⁾ Remap: TIMER1_CH0, TIMER1_ETI, PA15, SPI0_NSS |
| PC10 | 51 | I/O | 5VT | Default: PC10 Alternate: UART3_TX ⁽³⁾ Remap: USART2_TX ⁽⁶⁾ , SPI2_SCK ⁽³⁾ |
| PC11 | 52 | I/O | 5VT | Default: PC11 Alternate: UART3_RX ⁽³⁾ Remap: USART2_RX ⁽⁶⁾ , SPI2_MISO ⁽³⁾ |
| PC12 | 53 | I/O | 5VT | Default: PC12 Alternate: UART4_TX ⁽³⁾ Remap: USART2_CK ⁽⁶⁾ , SPI2_MOSI ⁽³⁾ |
| PD0 | 5 | I/O | 5VT | Default: PD0 |
| PD1 | 6 | I/O | 5VT | Default: PD1 |
| PD2 | 54 | I/O | 5VT | Default: PD2 Alternate: TIMER2_ETI, UART4_RX ⁽³⁾ |
| PB3 | 55 | I/O | 5VT | Default: JTDO Alternate: SPI2_SCK ⁽³⁾ Remap: PB3, TRACESWO, TIMER1_CH1, SPI0_SCK |
| PB4 | 56 | I/O | 5VT | Default: NJTRST Alternate: SPI2_MISO ⁽³⁾ Remap: TIMER2_CH0, PB4, SPI0_MISO |
| PB5 | 57 | I/O | | Default: PB5 Alternate: I2C0_SMBA, SPI2_MOSI ⁽³⁾ Remap: TIMER2_CH1, SPI0_MOSI |
| PB6 | 58 | I/O | 5VT | Default: PB6 |

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|-------------------|------|-------------------------|--------------------------|------------------------------------------------------------------------------------------------------|
| | | | | Alternate: I2C0_SCL, TIMER3_CH0 ⁽⁶⁾ , Remap: USART0_TX |
| PB7 | 59 | I/O | 5VT | Default: PB7 Alternate: I2C0_SDA, TIMER3_CH1 ⁽⁶⁾ Remap: USART0_RX |
| BOOT0 | 60 | I | | Default: BOOT0 |
| PB8 | 61 | I/O | 5VT | Default: PB8 Alternate: TIMER3_CH2 ⁽⁶⁾ , TIMER9_CH0 ⁽⁴⁾ Remap: I2C0_SCL |
| PB9 | 62 | I/O | 5VT | Default: PB9 Alternate: TIMER3_CH3 ⁽⁶⁾ , TIMER10_CH0 ⁽⁴⁾ Remap: I2C0_SDA |
| V _{SS_3} | 63 | P | | Default: V _{SS_3} |
| V _{DD_3} | 64 | P | | Default: V _{DD_3} |

Notes:

- (1) Type: I = input, O = output, P = power.
- (2) I/O Level: 5VT = 5 V tolerant.
- (3) Functions are available in GD32F101RC/D/E/F/G/I/K devices.
- (4) Functions are available in GD32F101RF/G/I/K devices.
- (5) In GD32F101RF/G/I/K devices, functions are fully available for ADC0 and ADC1; In GD32F101R4/6/8/B/C/D/E devices, functions are available for ADC0.
- (6) Functions are available in GD32F101R8/B/C/D/E/F/G/I/K devices.

2.6.4. GD32F101Cx LQFP48 pin definitions

Table 2-8. GD32F101Cx LQFP48 pin definitions

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|------------------|------|-------------------------|--------------------------|--------------------------------------------------------------------------------|
| V _{BAT} | 1 | P | | Default: V _{BAT} |
| PC13-TAMPER-RTC | 2 | I/O | | Default: PC13 Alternate: TAMPER-RTC |
| PC14-OSC32IN | 3 | I/O | | Default: PC14 Alternate: OSC32IN |
| PC15-OSC32OUT | 4 | I/O | | Default: PC15 Alternate: OSC32OUT |
| OSCIN | 5 | I | | Default: OSCIN Remap: PD0 |
| OSCOUT | 6 | O | | Default: OSCOUT Remap: PD1 |
| NRST | 7 | I/O | | Default: NRST |
| V _{SSA} | 8 | P | | Default: V _{SSA} |
| V _{DDA} | 9 | P | | Default: V _{DDA} |
| PA0-WKUP | 10 | I/O | | Default: PA0 Alternate: WKUP, USART1_CTS, ADC0_IN0, TIMER1_CH0, TIMER1_ETI |
| PA1 | 11 | I/O | | Default: PA1 Alternate: USART1_RTS, ADC0_IN1, TIMER1_CH1 |
| PA2 | 12 | I/O | | Default: PA2 Alternate: USART1_TX, ADC0_IN2, TIMER1_CH2 |
| PA3 | 13 | I/O | | Default: PA3 Alternate: USART1_RX, ADC0_IN3, TIMER1_CH3 |
| PA4 | 14 | I/O | | Default: PA4 Alternate: SPI0_NSS, USART1_CK, ADC0_IN4 |
| PA5 | 15 | I/O | | Default: PA5 Alternate: SPI0_SCK, ADC0_IN5 |
| PA6 | 16 | I/O | | Default: PA6 Alternate: SPI0_MISO, ADC0_IN6, TIMER2_CH0 |
| PA7 | 17 | I/O | | Default: PA7 Alternate: SPI0_MOSI, ADC0_IN7, TIMER2_CH1 |
| PB0 | 18 | I/O | | Default: PB0 Alternate: ADC0_IN8, TIMER2_CH2 |
| PB1 | 19 | I/O | | Default: PB1 Alternate: ADC0_IN9, TIMER2_CH3 |
| PB2 | 20 | I/O | 5VT | Default: PB2/BOOT1 |
| PB10 | 21 | I/O | 5VT | Default: PB10 Alternate: I2C1_SCL ⁽³⁾ , USART2_TX ⁽³⁾ |

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|-------------------|------|-------------------------|--------------------------|-----------------------------------------------------------------------------------------------------------|
| | | | | Remap: TIMER1_CH2 |
| PB11 | 22 | I/O | 5VT | Default: PB11 Alternate: I2C1_SDA ⁽³⁾ , USART2_RX ⁽³⁾ Remap: TIMER1_CH3 |
| V _{SS_1} | 23 | P | | Default: V _{SS_1} |
| V _{DD_1} | 24 | P | | Default: V _{DD_1} |
| PB12 | 25 | I/O | 5VT | Default: PB12 Alternate: SPI1_NSS ⁽³⁾ , I2C1_SMBA ⁽³⁾ , USART2_CK ⁽³⁾ |
| PB13 | 26 | I/O | 5VT | Default: PB13 Alternate: SPI1_SCK ⁽³⁾ , USART2_CTS ⁽³⁾ |
| PB14 | 27 | I/O | 5VT | Default: PB14 Alternate: SPI1_MISO ⁽³⁾ , USART2_RTS ⁽³⁾ |
| PB15 | 28 | I/O | 5VT | Default: PB15 Alternate: SPI1_MOSI ⁽³⁾ |
| PA8 | 29 | I/O | 5VT | Default: PA8 Alternate: USART0_CK, CK_OUT0 |
| PA9 | 30 | I/O | 5VT | Default: PA9 Alternate: USART0_TX |
| PA10 | 31 | I/O | 5VT | Default: PA10 Alternate: USART0_RX |
| PA11 | 32 | I/O | 5VT | Default: PA11 Alternate: USART0_CTS |
| PA12 | 33 | I/O | 5VT | Default: PA12 Alternate: USART0_RTS |
| PA13 | 34 | I/O | 5VT | Default: JTMS, SWDIO Remap: PA13 |
| V _{SS_2} | 35 | P | | Default: V _{SS_2} |
| V _{DD_2} | 36 | P | | Default: V _{DD_2} |
| PA14 | 37 | I/O | 5VT | Default: JTCK, SWCLK Remap: PA14 |
| PA15 | 38 | I/O | 5VT | Default: JTDI Remap: TIMER1_CH0, TIMER1_ETI, PA15, SPI0_NSS |
| PB3 | 39 | I/O | 5VT | Default: JTDO Remap: PB3, TRACESWO, TIMER1_CH1, SPI0_SCK |
| PB4 | 40 | I/O | 5VT | Default: NJTRST Remap: TIMER2_CH0, PB4, SPI0_MISO |
| PB5 | 41 | I/O | | Default: PB5 Alternate: I2C0_SMBA Remap: TIMER2_CH1, SPI0_MOSI |
| PB6 | 42 | I/O | 5VT | Default: PB6 Alternate: I2C0_SCL, TIMER3_CH0 ⁽³⁾ , Remap: USART0_TX |
| PB7 | 43 | I/O | 5VT | Default: PB7 |

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|-------------------|------|-------------------------|--------------------------|-------------------------------------------------------------------------|
| | | | | Alternate: I2C0_SDA , TIMER3_CH1 ⁽³⁾ Remap: USART0_RX |
| BOOT0 | 44 | I | | Default: BOOT0 |
| PB8 | 45 | I/O | 5VT | Default: PB8 Alternate: TIMER3_CH2 ⁽³⁾ Remap: I2C0_SCL |
| PB9 | 46 | I/O | 5VT | Default: PB9 Alternate: TIMER3_CH3 ⁽³⁾ Remap: I2C0_SDA |
| V _{SS_3} | 47 | P | | Default: V _{SS_3} |
| V _{DD_3} | 48 | P | | Default: V _{DD_3} |

Notes:

- (1) Type: I = input, O = output, P = power.
 (2) I/O Level: 5VT = 5 V tolerant.
 (3) Functions are available in GD32F101C8/B devices.

2.6.5. GD32F101Tx QFN36 pin definitions

Table 2-9. GD32F101Tx QFN36 pin definitions

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|-------------------|------|-------------------------|--------------------------|-------------------------------------------------------------------------------|
| OSCIN | 2 | I | | Default: OSCIN Remap: PD0 |
| OSCOUT | 3 | O | | Default: OSCOUT Remap: PD1 |
| NRST | 4 | I/O | | Default: NRST |
| V _{SSA} | 5 | P | | Default: V _{SSA} |
| V _{DDA} | 6 | P | | Default: V _{DDA} |
| PA0-WKUP | 7 | I/O | | Default: PA0 Alternate: WKUP, USART1_CTS, ADC0_IN0, TIMER1_CH0, TIMER1_ETI |
| PA1 | 8 | I/O | | Default: PA1 Alternate: USART1_RTS, ADC0_IN1, TIMER1_CH1 |
| PA2 | 9 | I/O | | Default: PA2 Alternate: USART1_TX, ADC0_IN2, TIMER1_CH2 |
| PA3 | 10 | I/O | | Default: PA3 Alternate: USART1_RX, ADC0_IN3, TIMER1_CH3 |
| PA4 | 11 | I/O | | Default: PA4 Alternate: SPI0_NSS, USART1_CK, ADC0_IN4 |
| PA5 | 12 | I/O | | Default: PA5 Alternate: SPI0_SCK, ADC0_IN5 |
| PA6 | 13 | I/O | | Default: PA6 Alternate: SPI0_MISO, ADC0_IN6, TIMER2_CH0 |
| PA7 | 14 | I/O | | Default: PA7 Alternate: SPI0_MOSI, ADC0_IN7, TIMER2_CH1 |
| PB0 | 15 | I/O | | Default: PB0 Alternate: ADC0_IN8, TIMER2_CH2 |
| PB1 | 16 | I/O | | Default: PB1 Alternate: ADC0_IN9, TIMER2_CH3 |
| PB2 | 17 | I/O | 5VT | Default: PB2/BOOT1 |
| V _{SS_1} | 18 | P | | Default: V _{SS_1} |
| V _{DD_1} | 19 | P | | Default: V _{DD_1} |
| PA8 | 20 | I/O | 5VT | Default: PA8 Alternate: USART0_CK, CK_OUT0 |
| PA9 | 21 | I/O | 5VT | Default: PA9 Alternate: USART0_TX |
| PA10 | 22 | I/O | 5VT | Default: PA10 Alternate: USART0_RX |
| PA11 | 23 | I/O | 5VT | Default: PA11 Alternate: USART0_CTS |

| Pin Name | Pins | Pin Type ⁽¹⁾ | I/O Level ⁽²⁾ | Functions description |
|-------------------|------|-------------------------|--------------------------|------------------------------------------------------------------------------------|
| PA12 | 24 | I/O | 5VT | Default: PA12 Alternate: USART0_RTS |
| PA13 | 25 | I/O | 5VT | Default: JTMS, SWDIO Remap: PA13 |
| V _{SS_2} | 26 | P | | Default: V _{SS_2} |
| V _{DD_2} | 27 | P | | Default: V _{DD_2} |
| PA14 | 28 | I/O | 5VT | Default: JTCK, SWCLK Remap: PA14 |
| PA15 | 29 | I/O | 5VT | Default: JTDI Remap: TIMER1_CH0, TIMER1_ETI, PA15, SPI0_NSS |
| PB3 | 30 | I/O | 5VT | Default: JTDO Remap: PB3, TRACESWO, TIMER1_CH1, SPI0_SCK |
| PB4 | 31 | I/O | 5VT | Default: NJTRST Remap: TIMER2_CH0, PB4, SPI0_MISO |
| PB5 | 32 | I/O | | Default: PB5 Alternate: I2C0_SMBA Remap: TIMER2_CH1, SPI0_MOSI |
| PB6 | 33 | I/O | 5VT | Default: PB6 Alternate: I2C0_SCL, TIMER3_CH0 ⁽³⁾ Remap: USART0_TX |
| PB7 | 34 | I/O | 5VT | Default: PB7 Alternate: I2C0_SDA, TIMER3_CH1 ⁽³⁾ Remap: USART0_RX |
| BOOT0 | 35 | I | | Default: BOOT0 |
| V _{SS_3} | 36 | P | | Default: V _{SS_3} |
| V _{DD_3} | 1 | P | | Default: V _{DD_3} |

Notes:

- (1) Type: I = input, O = output, P = power.
 (2) I/O Level: 5VT = 5 V tolerant.
 (3) Functions are available in GD32F101T8/B devices.

3. Functional description

3.1. ARM® Cortex™-M3 core

The Cortex™-M3 processor is the latest generation of ARM® processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

- 32-bit ARM® Cortex™-M3 processor core
- Up to 56 MHz operation frequency
- Single-cycle multiplication and hardware divider
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex™-M3 processor is based on the ARMv7 architecture and supports both Thumb and Thumb-2 instruction sets. Some system peripherals listed below are also provided by Cortex™-M3:

- Internal Bus Matrix connected with I-Code bus, D-Code bus, System bus, Private Peripheral Bus (PPB) and debug accesses.
- Nested Vectored Interrupt Controller (NVIC).
- Flash Patch and Breakpoint (FPB).
- Data Watchpoint and Trace (DWT).
- Instrumentation Trace Macrocell (ITM).
- Embedded Trace Macrocell (ETM).
- Serial Wire JTAG Debug Port (SWJ-DP).
- Trace Port Interface Unit (TPIU).
- Memory Protection Unit (MPU).

3.2. On-chip memory

- Up to 3072 Kbytes of Flash memory
- Up to 80 Kbytes of SRAM

The ARM® Cortex™-M3 processor is structured in Harvard architecture which can use separate buses to fetch instructions and load/store data. 3072 Kbytes of inner Flash and 80 Kbytes of inner SRAM at most is available for storing programs and data, both accessed (R/W) at CPU clock speed with zero wait states. The [Table 2-4. GD32F101xx memory map](#) shows the memory map of the GD32F101xx series of devices, including code, SRAM, peripheral, and other pre-defined regions.

3.3. Clock, reset and supply management

- Internal 8 MHz factory-trimmed RC and external 4 to 16 MHz crystal oscillator
- Internal 40 KHz RC calibrated oscillator and external 32.768 KHz crystal oscillator
- Integrated system clock PLL
- 2.6 to 3.6 V application supply and I/Os
- Supply Supervisor: POR (Power On Reset), PDR (Power Down Reset), and low voltage detector (LVD)

The Clock Control unit provides a range of frequencies and clock functions. These include an Internal 8M RC oscillator (IRC8M), a High Speed crystal oscillator (HXTAL), a Low Speed Internal 40K RC oscillator (IRC40K), a Low Speed crystal oscillator (LXTAL), a Phase Lock Loop (PLL), a HXTAL clock monitor, clock prescalers, clock multiplexers and clock gating circuitry. The frequency of AHB, APB2 and the APB1 domains can be configured by each prescaler. The maximum frequency of the AHB, APB2 and APB1 domains is 56 MHz/56 MHz/56 MHz. See [Figure 2-8. GD32F101xx clock tree](#) for details on the clock tree.

GD32F10x Reset Control includes the control of three kinds of reset: power reset, system reset and backup domain reset. The system reset resets the processor core and peripheral IP components except for the SW-DP controller and the Backup domain. Power-on reset (POR) and power-down reset (PDR) are always active, and ensures proper operation starting from/down to 2.6 V. The device remains in reset mode when V_{DD} is below a specified threshold. The embedded low voltage detector (LVD) monitors the power supply, compares it to the voltage threshold and generates an interrupt as a warning message for leading the MCU into security.

Power supply schemes:

- V_{DD} range: 2.6 to 3.6 V, external power supply for I/Os and the internal regulator. Provided externally through V_{DD} pins.
- V_{SSA} , V_{DDA} range: 2.6 to 3.6 V, external analog power supplies for ADC, reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} , respectively.
- V_{BAT} range: 1.8 to 3.6 V, power supply for RTC, external clock 32 KHz oscillator and backup registers (through power switch) when V_{DD} is not present.

3.4. Boot modes

At startup, boot pins are used to select one of three boot options:

- Boot from main flash memory (default)
- Boot from system memory
- Boot from on-chip SRAM

The boot loader is located in the internal boot ROM memory (system memory). It is used to reprogram the Flash memory by using USART0 (PA9 and PA10), if devices are GD32F101xF/G/I/K, USART1 (PA2 and PA3) is also available for boot functions. It also can

be used to transfer and update the Flash memory code, the data and the vector table sections. In default condition, boot from bank 0 of Flash memory is selected. It also supports to boot from bank 1 of Flash memory by setting a bit in option bytes.

3.5. Power saving modes

The MCU supports three kinds of power saving modes to achieve even lower power consumption. They are sleep mode, deep-sleep mode, and standby mode. These operating modes reduce the power consumption and allow the application to achieve the best balance between the CPU operating time, speed and power consumption.

- **Sleep mode**

In sleep mode, only clock of Cortex™-M3 is off. All peripherals continue to operate and any interrupt/event can wake up the system.

- **Deep-sleep mode**

In deep-sleep mode, all clocks in the 1.2V domain are off, and all of IRC8M, HXTAL and PLLs are disabled. Only the contents of SRAM and registers are retained. Any interrupt or wakeup event from EXTI lines can wake up the system from the deep-sleep mode including the 16 external lines, the RTC alarm, the LVD output, USB Wakeup and Ethernet Wakeup. When exiting the deep-sleep mode, the IRC8M is selected as the system clock.

- **Standby mode**

In standby mode, the whole 1.2V domain is power off, the LDO is shut down, and all of IRC8M, HXTAL and PLL are disabled. The contents of SRAM and registers (except Backup registers) are lost. There are four wakeup sources for the Standby mode, including the external reset from NRST pin, the RTC alarm, the FWDGT reset, and the rising edge on WKUP pin.

3.6. Analog to digital converter (ADC)

- 12-bit SAR ADC engine
- Up to 1 MSPS for 12-bit resolution
- Conversion range: V_{SSA} to V_{DDA} (2.6 to 3.6 V)
- Temperature sensor

Up to two 12-bit 1 μ s multi-channel ADCs are integrated in the device. Each is a total of up to 16 multiplexed external channels. An analog watchdog block can be used to detect the channels, which are required to remain within a specific threshold window. A configurable channel management block of analog inputs also can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced usages.

The ADCs can be triggered from the events generated by the general timers (TIMERx) with internal connection. The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between $2.6\text{ V} < V_{DDA} < 3.6\text{ V}$. The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

3.7. DMA

- 7 channel DMA0 controller and 5 channel DMA1 controller
- Peripherals supported: Timers, ADC, SPIs, I2Cs, USARTs

The direct memory access (DMA) controllers provide a hardware method of transferring data between peripherals and/or memory without intervention from the CPU, thereby freeing up bandwidth for other system functions. Three types of access method are supported: peripheral to memory, memory to peripheral, memory to memory.

Each channel is connected to fixed hardware DMA requests. The priorities of DMA channel requests are determined by software configuration and hardware channel number. Transfer size of source and destination are independent and configurable.

3.8. General-purpose inputs/outputs (GPIOs)

- Up to 112 fast GPIOs, all mappable on 16 external interrupt lines
- Analog input/output configurable
- Alternate function input/output configurable

There are up to 112 general purpose I/O pins (GPIO), named PA0 ~ PA15, PB0 ~ PB15, PC0 ~ PC15, PD0 ~ PD15, PE0 ~ PE15, PF0 ~ PF15 and PG0 ~ PG15 for the device to implement logic input/output functions. Each GPIO port has related control and configuration registers to satisfy the requirements of specific applications. The external interrupt on the GPIO pins of the device have related control and configuration registers in the Interrupt/event Controller Unit (EXTI). The GPIO ports are pin-shared with other alternative functions (AFs) to obtain maximum flexibility on the package pins. The GPIO pins can be used as alternative functional pins by configuring the corresponding registers regardless of the AF input or output pins. Each of the GPIO pins can be configured by software as output (push-pull or open-drain), input, peripheral alternate function or analog mode. Each GPIO pin can be configured as pull-up, pull-down or no pull-up/pull-down. All GPIOs are high-current capable except for analog mode.

3.9. Timers and PWM generation

- Up to ten 16-bit general timers, and two 16-bit basic timer (TIMER5 & TIMER6)
- Up to 4 independent channels of PWM, output compare or input capture for each general timer and external trigger input
- Encoder interface controller with two inputs using quadrature decoder
- 24-bit SysTick timer down counter
- 2 watchdog timers (Free watchdog timer and window watchdog timer)

The general timer, known as TIMER1 ~ TIMER4, TIMER8 ~ TIMER10, TIMER11 ~ TIMER13 can be used for a variety of purposes including general time, input signal pulse width measurement or output waveform generation such as a single pulse generation or PWM

output, up to 4 independent channels for input capture/output compare. The general timer also supports an encoder interface with two inputs using quadrature decoder.

The basic timer, known as TIMER5 and TIMER6, are mainly used to generate analog trigger and can also be used as simple 16-bit time base.

The GD32F101xx have two watchdog peripherals, free watchdog timer and window watchdog timer. They offer a combination of high safety level, flexibility of use and timing accuracy.

The free watchdog timer consists of an 8-stage prescaler and a 12-bit down-counter, it is clocked from an independent 40 KHz internal RC and as it operates independently of the main clock, it can operate in deep-sleep and standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management.

The window watchdog timer is based on a 7-bit down counter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early wakeup interrupt capability and the counter can be frozen in debug mode.

The SysTick timer is dedicated for OS, but could also be used as a standard down counter. The features are shown below:

- A 24-bit down counter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source

3.10. Real time clock (RTC)

- 32-bit up-counter with a programmable 20-bit prescaler
- Alarm function
- Interrupt and wake-up event

The real time clock is an independent timer which provides a set of continuously running counters which can be used with suitable software to provide a clock calendar function, and provides an alarm interrupt and an expected interrupt. The RTC features a 32-bit programmable counter for long-term measurement using the compare register to generate an alarm. A 20-bit prescaler is used for the time base clock and is by default configured to generate a time base of 1 second from a clock at 32.768 KHz from external crystal oscillator.

3.11. Inter-integrated circuit (I2C)

- Up to two I2C bus interfaces can support both master and slave mode with a frequency up to 400 KHz
- Provide arbitration function, optional PEC (packet error checking) generation and

checking

- Supports 7-bit and 10-bit addressing mode and general call addressing mode

The I2C interface is an internal circuit allowing communication with an external I2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I2C module provides transfer rate of up to 100 KHz in standard mode and up to 400 KHz in fast mode. The I2C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I2C bus at the same time. A CRC-8 calculator is also provided in I2C interface to perform packet error checking for I2C data.

3.12. Serial peripheral interface (SPI)

- Up to three SPI interfaces with a frequency of up to 18 MHz
- Support both master and slave mode
- Hardware CRC calculation and transmit automatic CRC error checking

The SPI interface uses 4 pins, among which are the serial data input and output lines (MISO & MOSI), the clock line (SCK) and the slave select line (NSS). Both SPIs can be served by the DMA controller. The SPI interface may be used for a variety of purposes, including simplex synchronous transfers on two lines with a possible bidirectional data line or reliable communication using CRC checking.

3.13. Universal synchronous asynchronous receiver transmitter (USART)

- Up to three USARTs and two UARTs with operating frequency up to 3.5 MHz
- Supports both asynchronous and clocked synchronous serial communication modes
- IrDA SIR encoder and decoder support
- LIN break generation and detection
- USARTs support ISO 7816-3 compliant smart card interface

The USART (USART0, USART1 and USART2) and UART (UART3 & UART4) are used to translate data between parallel and serial interfaces, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. It is also commonly used for RS-232 standard communication. The USART includes a programmable baud rate generator which is capable of dividing the system clock to produce a dedicated clock for the USART transmitter and receiver. The USART also supports DMA function for high speed data communication except UART4.

3.14. External memory controller (EXMC)

- Supported external memory: SRAM, PSRAM, ROM and NOR-Flash, NAND Flash and CF card
- Up to 16-bit data bus
- Support to interface with Motorola 6800 and Intel 8080 type LCD directly

External memory controller (EXMC) is an abbreviation of external memory controller. It is divided in to several sub-banks for external device support, each sub-bank has its own chip selection signal but at one time, only one bank can be accessed. The EXMC support code execution from external memory except NAND Flash and CF card. The EXMC also can be configured to interface with the most common LCD module of Motorola 6800 and Intel 8080 series and reduce the system cost and complexity.

3.15. Debug mode

- Serial wire JTAG debug port (SWJ-DP)

The ARM® SWJ-DP Interface is embedded and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

3.16. Package and operation temperature

- LQFP144 (GD32F101Zx), LQFP100 (GD32F101Vx), LQFP64 (GD32F101Rx), LQFP48 (GD32F101Cx) and QFN36 (GD32F101Tx)
- Operation temperature range: -40°C to +85°C (industrial level)

4. Electrical characteristics

4.1. Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-1. Absolute maximum ratings

| Symbol | Parameter | Min | Max | Unit |
|-----------|----------------------------------|-----------------|-----------------|------|
| V_{DD} | External voltage range | $V_{SS} - 0.3$ | $V_{SS} + 3.6$ | V |
| V_{DDA} | External analog supply voltage | $V_{SSA} - 0.3$ | $V_{SSA} + 3.6$ | V |
| V_{BAT} | External battery supply voltage | $V_{SS} - 0.3$ | $V_{SS} + 3.6$ | V |
| V_{IN} | Input voltage on 5V tolerant pin | $V_{SS} - 0.3$ | $V_{DD} + 4.0$ | V |
| | Input voltage on other I/O | $V_{SS} - 0.3$ | 4.0 | V |
| I_{IO} | Maximum current for GPIO pins | — | 25 | mA |
| T_A | Operating temperature range | -40 | +85 | °C |
| T_{STG} | Storage temperature range | -55 | +150 | °C |
| T_J | Maximum junction temperature | — | 125 | °C |

4.2. Recommended DC characteristics

Table 4-2. DC operating conditions

| Symbol | Parameter | Conditions | Min | Typ. | Max | Unit |
|-----------|------------------------|------------------|-----|------|-----|------|
| V_{DD} | Supply voltage | — | 2.6 | 3.3 | 3.6 | V |
| V_{DDA} | Analog supply voltage | Same as V_{DD} | 2.6 | 3.3 | 3.6 | V |
| V_{BAT} | Battery supply voltage | — | 1.8 | — | 3.6 | V |

4.3. Power consumption

The power measurements specified in the tables represent that code with data executing from on-chip Flash with the following specifications.

Table 4-3. Power consumption characteristics (for GD32F101x4/6/8/B devices)

| Symbol | Parameter | Conditions | Min | Typ. | Max | Unit |
|-----------------------------------------------------------------------------------------------|----------------------------------|-------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------|-------|-------|------|
| I _{DD} | Supply current (Run mode) | V _{DD} =V _{BAT} =3.3V, HXTAL=8MHz, System clock=56 MHz, all peripherals enabled | — | 21.42 | — | mA |
| | | V _{DD} =V _{BAT} =3.3V, HXTAL=8MHz, System clock =56 MHz, all peripherals disabled | — | 16.55 | — | mA |
| | | V _{DD} =V _{BAT} =3.3V, HXTAL=8MHz, System clock =36MHz, all peripherals enabled | — | 15.48 | — | mA |
| | | V _{DD} =V _{BAT} =3.3V, HXTAL=8MHz, System Clock =36 MHz, all peripherals disabled | — | 11.5 | — | mA |
| | Supply current (Sleep mode) | V _{DD} =V _{BAT} =3.3V, HXTAL=8MHz, System clock =56 MHz, CPU clock off, all peripherals enabled | — | 9.93 | — | mA |
| | | V _{DD} =V _{BAT} =3.3V, HXTAL=8MHz, System clock =56 MHz, CPU clock off, all peripherals disabled | — | 4.02 | — | mA |
| | Supply current (Deep-Sleep mode) | V _{DD} =V _{BAT} =3.3V, All clock off, regulator in run mode, IRC40K on, RTC on, all GPIOs analog mode | — | 356.9 | — | μA |
| | | V _{DD} =V _{BAT} =3.3V, All clock off, regulator in low power mode, IRC40K on, RTC on, all GPIOs analog mode | — | 346.7 | — | μA |
| | Supply current (Standby mode) | V _{DD} =V _{BAT} =3.3V, LDO off, LXTAL off, IRC40K on, RTC on | — | 9.52 | — | μA |
| | | V _{DD} =V _{BAT} =3.3V, LDO off, LXTAL off, IRC40K on, RTC off | — | 9.17 | — | μA |
| | | V _{DD} =V _{BAT} =3.3V, LDO off, LXTAL off, IRC40K off, RTC off | — | 7.87 | — | μA |
| | I _{BAT} | Battery supply current (Standby mode) | V _{DD} not available, V _{BAT} =3.6V, LDO off, LXTAL on, IRC40K off, RTC on | — | 13.17 | — |
| V _{DD} not available, V _{BAT} =3.3 V, LDO off, LXTAL off, IRC40K on, RTC on | | | — | 10.41 | — | μA |
| V _{DD} not available, V _{BAT} =2.6 V, LDO off, LXTAL off, IRC40K on, RTC on | | | — | 5.9 | — | μA |
| t _{SLEEP} | Wakeup from Sleep mode | system clock = IRC8M = 8MHz | — | 4.5 | — | μs |
| t _{DEEPSLEEP} | Wakeup from deep-sleep mode | system clock = IRC8M = 8MHz | — | 6.5 | — | μs |

| | | | | | | |
|--------|--------------------------------------------------------------|-----------------------------|---|------|---|----|
| | (regulator in run mode) | | | | | |
| | Wakeup from deep-sleep mode (regulator in low power mode) | system clock = IRC8M = 8MHz | — | 6.5 | — | μs |
| tSTDBY | Wakeup from Standby mode | system clock = IRC8M = 8MHz | — | 59.4 | — | ms |

Table 4-4. Power consumption characteristics (for GD32F101xC/D/E/F/G//K devices)

| Symbol | Parameter | Conditions | Min | Typ. | Max | Unit |
|-----------------------------------------------------------------------------------------------|----------------------------------|-------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------|-------|-------|------|
| I _{DD} | Supply current (Run mode) | V _{DD} =V _{BAT} =3.3V, HXTAL=8MHz, System clock=56 MHz, all peripherals enabled | — | 27.09 | — | mA |
| | | V _{DD} =V _{BAT} =3.3V, HXTAL=8MHz, System clock =56 MHz, all peripherals disabled | — | 20.23 | — | mA |
| | | V _{DD} =V _{BAT} =3.3V, HXTAL=8MHz, System clock =36MHz, all peripherals enabled | — | 19.43 | — | mA |
| | | V _{DD} =V _{BAT} =3.3V, HXTAL=8MHz, System Clock =36 MHz, all peripherals disabled | — | 13.89 | — | mA |
| | Supply current (Sleep mode) | V _{DD} =V _{BAT} =3.3V, HXTAL=8MHz, System clock =56 MHz, CPU clock off, all peripherals enabled | — | 14.29 | — | mA |
| | | V _{DD} =V _{BAT} =3.3V, HXTAL=8MHz, System clock =56 MHz, CPU clock off, all peripherals disabled | — | 4.94 | — | mA |
| | Supply current (Deep-Sleep mode) | V _{DD} =V _{BAT} =3.3V, All clock off, regulator in run mode, IRC40K on, RTC on, all GPIOs analog mode | — | 666.2 | — | μA |
| | | V _{DD} =V _{BAT} =3.3V, All clock off, regulator in low power mode, IRC40K on, RTC on, all GPIOs analog mode | — | 657.7 | — | μA |
| | Supply current (Standby mode) | V _{DD} =V _{BAT} =3.3V, LDO off, LXTAL off, IRC40K on, RTC on | — | 9.68 | — | μA |
| | | V _{DD} =V _{BAT} =3.3V, LDO off, LXTAL off, IRC40K on, RTC off | — | 9.3 | — | μA |
| | | V _{DD} =V _{BAT} =3.3V, LDO off, LXTAL off, IRC40K off, RTC off | — | 8.05 | — | μA |
| | I _{BAT} | Battery supply current (Standby mode) | V _{DD} not available, V _{BAT} =3.6V, LDO off, LXTAL on, IRC40K off, RTC on | — | 12.73 | — |
| V _{DD} not available, V _{BAT} =3.3 V, LDO off, LXTAL off, IRC40K on, RTC on | | | — | 10.02 | — | μA |
| V _{DD} not available, V _{BAT} =2.6 V, LDO off, LXTAL off, IRC40K on, RTC on | | | — | 5.59 | — | μA |

| | | | | | | |
|-----------------|-----------------------------------------------------------|-----------------------------|---|-------|---|---------|
| t_{SLEEP} | Wakeup from Sleep mode | system clock = IRC8M = 8MHz | — | 4.5 | — | μs |
| $t_{DEEPSLEEP}$ | Wakeup from deep-sleep mode (regulator in run mode) | system clock = IRC8M = 8MHz | — | 6 | — | μs |
| | Wakeup from deep-sleep mode (regulator in low power mode) | system clock = IRC8M = 8MHz | — | 6 | — | μs |
| t_{STDBY} | Wakeup from Standby mode | system clock = IRC8M = 8MHz | — | 118.8 | — | ms |

4.4. EMC characteristics

EMS (electromagnetic susceptibility) includes ESD (Electrostatic discharge, positive and negative) and FTB (Burst of Fast Transient voltage, positive and negative) testing result is given in the [Table 4-5. EMS characteristics](#), based on the EMS levels and classes compliant with IEC 61000 series standard.

Table 4-5. EMS characteristics

| Symbol | Parameter | Conditions | Level/Class |
|------------------|------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------|-------------|
| V _{ESD} | Voltage applied to all device pins to induce a functional disturbance | V _{DD} = 3.3 V, T _A = +25 °C conforms to IEC 61000-4-2 | 3B |
| V _{FTB} | Fast transient voltage burst applied to induce a functional disturbance through 100 pF on V _{DD} and V _{SS} pins | V _{DD} = 3.3 V, T _A = +25 °C conforms to IEC 61000-4-4 | 4A |

EMI (Electromagnetic Interference) emission testing result is given in the [Table 4-6. EMI characteristics](#), compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 4-6. EMI characteristics

| Symbol | Parameter | Conditions | Tested frequency band | Conditions | | | Unit |
|------------------|------------|---------------------------------------------------------------------------------------|-----------------------|------------|------|------|------|
| | | | | 8M | 36M | 56M | |
| S _{EMI} | Peak level | V _{DD} = 3.3 V, T _A = +25 °C, compliant with IEC 61967-2 | 0.1 to 2 MHz | <0 | <0 | <0 | dBμV |
| | | | 2 to 30 MHz | -5.3 | -4.1 | -3.7 | |
| | | | 30 to 130 MHz | -8.5 | -7 | -6.5 | |
| | | | 130 MHz to 1GHz | -8 | -7 | -7 | |

4.5. Power supply supervisor characteristics

Table 4-7. Power supply supervisor characteristics (for GD32F101x4/6/8/B devices)

| Symbol | Parameter | Conditions | Min | Typ. | Max | Unit |
|----------------------|----------------------------|------------|------|------|------|------|
| V _{POR} | Power on reset threshold | — | 2.32 | 2.40 | 2.48 | V |
| V _{PDR} | Power down reset threshold | — | 2.27 | 2.35 | 2.43 | V |
| V _{HYST} | PDR hysteresis | — | — | 0.05 | — | V |
| T _{RSTTEMP} | Reset temporization | — | — | 2 | — | ms |

Table 4-8. Power supply supervisor characteristics (for GD32F101xC/D/E/F/G/I/K devices)

| Symbol | Parameter | Conditions | Min | Typ. | Max | Unit |
|--------|-----------|------------|-----|------|-----|------|
|--------|-----------|------------|-----|------|-----|------|

| | | | | | | |
|----------------------|----------------------------|---|------|------|------|----|
| V _{POR} | Power on reset threshold | — | 2.27 | 2.40 | 2.43 | V |
| V _{PDR} | Power down reset threshold | — | — | 1.90 | — | V |
| V _{HYST} | PDR hysteresis | — | — | 0.5 | — | V |
| T _{RSTTEMP} | Reset temporization | — | — | 2 | — | ms |

4.6. Electrical sensitivity

The device is strained in order to determine its performance in terms of electrical sensitivity. Electrostatic discharges (ESD) are applied directly to the pins of the sample. Static latch-up (LU) test is based on the two measurement methods.

Table 4-9. ESD characteristics

| Symbol | Parameter | Conditions | Min | Typ. | Max | Unit |
|----------------|-------------------------------------------------------|----------------------------------------------|-----|------|------|------|
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | $T_A=25\text{ }^\circ\text{C}$; JESD22-A114 | — | — | 4000 | V |
| $V_{ESD(CDM)}$ | Electrostatic discharge voltage (charge device model) | $T_A=25\text{ }^\circ\text{C}$; JESD22-C101 | — | — | 1000 | V |

Table 4-10. Static latch-up characteristics

| Symbol | Parameter | Conditions | Min | Typ. | Max | Unit |
|--------|----------------------------------|-----------------------------------------|-----|------|-----------|------|
| LU | I-test | $T_A=25\text{ }^\circ\text{C}$; JESD78 | — | — | ± 100 | mA |
| | V_{supply} over voltage | | — | — | 5.4 | V |

4.7. External clock characteristics

Table 4-11. High speed external clock (HXTAL) generated from a crystal/ceramic characteristics

| Symbol | Parameter | Conditions | Min | Typ. | Max | Unit |
|----------------------|-------------------------------------------------------------------|-----------------------------------------------------------------|-----|------|-----|---------------|
| f_{HXTAL} | High Speed External oscillator (HXTAL) frequency | $V_{\text{DD}}=3.3\text{V}$ | 3 | 8 | 32 | MHz |
| C_{HXTAL} | Recommended load capacitance on OSCIN and OSCOUT | — | — | 20 | 30 | pF |
| R_{FHXTAL} | Recommended external feedback resistor between XTALIN and XTALOUT | — | — | 1 | — | M Ω |
| D_{HXTAL} | HXTAL oscillator duty cycle | — | 48 | 50 | 52 | % |
| I_{DDHXTAL} | HXTAL oscillator operating current | $V_{\text{DD}}=3.3\text{V}$, $T_{\text{A}}=25^{\circ}\text{C}$ | — | 1.4 | — | μA |
| t_{SUHXTAL} | HXTAL oscillator startup time | $V_{\text{DD}}=3.3\text{V}$, $T_{\text{A}}=25^{\circ}\text{C}$ | — | 2 | — | ms |

Table 4-12. Low speed external clock (LXTAL) generated from a crystal/ceramic characteristics

| Symbol | Parameter | Conditions | Min | Typ. | Max | Unit |
|----------------------|-----------------------------------------------------------------------|--------------------------------------------|-----|--------|------|---------------|
| f_{LXTAL} | Low Speed External oscillator (LXTAL) frequency | $V_{\text{DD}}=V_{\text{BAT}}=3.3\text{V}$ | — | 32.768 | 1000 | KHz |
| C_{LXTAL} | Recommended load capacitance on OSC32IN and OSC32OUT | — | — | — | 15 | pF |
| R_{FLXTAL} | Recommended external feedback resistor between XTAL32IN and XTAL32OUT | — | — | 5 | — | M Ω |
| D_{LXTAL} | LXTAL oscillator duty cycle | — | 48 | 50 | 52 | % |
| I_{DDLXTAL} | LXTAL oscillator operating current | $V_{\text{DD}}=V_{\text{BAT}}=3.3\text{V}$ | — | 1.4 | — | μA |
| t_{SULXTAL} | LXTAL oscillator startup time | $V_{\text{DD}}=V_{\text{BAT}}=3.3\text{V}$ | — | 3 | — | s |

4.8. Internal clock characteristics

Table 4-13. High speed internal clock (IRC8M) characteristics

| Symbol | Parameter | Conditions | Min | Typ. | Max | Unit |
|---------------|-----------------------------------------------------|----------------------------------------------------|------|------|------|---------|
| f_{IRC8M} | High Speed Internal Oscillator (IRC8M) frequency | $V_{DD}=3.3V$ | — | 8 | — | MHz |
| ACC_{IRC8M} | IRC8Moscillator frequency accuracy, factory-trimmed | $V_{DD}=3.3V, T_A=-40^{\circ}C \sim +105^{\circ}C$ | -2.5 | — | +1.5 | % |
| | | $V_{DD}=3.3V, T_A=0^{\circ}C \sim +85^{\circ}C$ | -1.2 | — | +1.2 | % |
| | | $V_{DD}=3.3V, T_A=25^{\circ}C$ | -1 | — | +1 | % |
| D_{IRC8M} | IRC8Moscillator duty cycle | $V_{DD}=3.3V, f_{IRC8M}=8MHz$ | 48 | 50 | 52 | % |
| $I_{DDIRC8M}$ | IRC8Moscillator operating current | $V_{DD}=3.3V, f_{IRC8M}=8MHz$ | — | 80 | 100 | μA |
| $t_{SUIRC8M}$ | IRC8Moscillator startup time | $V_{DD}=3.3V, f_{IRC8M}=8MHz$ | 1 | — | 2 | μs |

Table 4-14. Low speed internal clock (IRC40K) characteristics

| Symbol | Parameter | Conditions | Min | Typ. | Max | Unit |
|----------------|--------------------------------------------------|-----------------------------------------------------------|-----|------|-----|---------|
| f_{IRC40K} | Low Speed Internal oscillator (IRC40K) frequency | $V_{DD}=V_{BAT}=3.3V, T_A=-40^{\circ}C \sim +85^{\circ}C$ | 30 | 40 | 60 | KHz |
| $I_{DDIRC40K}$ | IRC40Koscillator operating current | $V_{DD}=V_{BAT}=3.3V, T_A=25^{\circ}C$ | — | 1 | 2 | μA |
| $t_{SUIRC40K}$ | IRC40Koscillator startup time | $V_{DD}=V_{BAT}=3.3V, T_A=25^{\circ}C$ | — | — | 80 | μs |

4.9. PLL characteristics

Table 4-15. PLL characteristics

| Symbol | Parameter | Conditions | Min | Typ. | Max | Unit |
|-------------|----------------------------|------------|-----|------|-----|---------|
| f_{PLLIN} | PLL input clock frequency | | 1 | 8 | 25 | MHz |
| f_{PLL} | PLL output clock frequency | | 16 | — | 56 | MHz |
| t_{LOCK} | PLL lock time | | — | — | 100 | μs |

4.10. Memory characteristics

Table 4-16. Flash memory characteristics

| Symbol | Parameter | Conditions | Min | Typ. | Max | Unit |
|--------------|----------------------------------------------------------------------|--------------------------------------|-----|------|-----|---------|
| PE_{CYC} | Number of guaranteed program/erase cycles before failure (Endurance) | $T_A=-40^{\circ}C \sim +85^{\circ}C$ | 100 | — | — | kcycles |
| t_{RET} | Data retention time | $T_A=125^{\circ}C$ | 20 | — | — | years |
| t_{PROG} | Word programming time | $T_A=-40^{\circ}C \sim +85^{\circ}C$ | 200 | — | 400 | μs |
| t_{ERASE} | Page erase time | $T_A=-40^{\circ}C \sim +85^{\circ}C$ | 60 | 100 | 450 | ms |
| t_{MERASE} | Mass erase time | $T_A=-40^{\circ}C \sim +85^{\circ}C$ | 3.2 | — | 9.6 | s |

4.11. GPIO characteristics

Table 4-17. I/O port characteristics (for GD32F101x4/6/8/B devices)

| Symbol | Parameter | Conditions | Min | Typ. | Max | Unit |
|-----------------|-------------------------------------------------------------------|----------------------------------|----------------------------|------|----------------------------|------|
| V _{IL} | Standard IO Low level input voltage | 2.6V ≤ V _{DD} ≤ 3.6V | -0.3 | — | 0.35 V _{DD} -0.06 | V |
| | 5V-tolerant IO Low level input voltage | 2.6V ≤ V _{DD} ≤ 3.6V | -0.3 | — | 0.4 V _{DD} -0.04 | V |
| V _{IH} | Standard IO High level input voltage | 2.6V ≤ V _{DD} ≤ 3.6V | 0.6 V _{DD} +0.14 | — | V _{DD} +0.3 | V |
| | 5V-tolerant IO High level input voltage | 2.6V ≤ V _{DD} ≤ 3.6V | 0.45 V _{DD} +0.13 | — | 5.5 | V |
| V _{OL} | Output low level voltage for an IO pin (I _{IO} = +8mA) | 2.6V ≤ V _{DD} ≤ 3.6V | — | — | 0.2 | V |
| V _{OH} | Output high level voltage for an IO pin (I _{IO} = +8mA) | 2.6V ≤ V _{DD} ≤ 3.6V | V _{DD} -0.2 | — | — | V |
| V _{OL} | Output low level voltage for an IO pin (I _{IO} = +20mA) | 2.6V ≤ V _{DD} ≤ 3.6V | — | — | 0.5 | V |
| V _{OH} | Output high level voltage for an IO pin (I _{IO} = +20mA) | 2.6V ≤ V _{DD} ≤ 3.6V | V _{DD} -0.5 | — | — | V |
| R _{PU} | Internal pull-up resistor | V _{IN} =V _{SS} | 30 | 40 | 50 | kΩ |
| R _{PD} | Internal pull-down resistor | V _{IN} =V _{DD} | 30 | 40 | 50 | kΩ |

Table 4-18. I/O port characteristics (for GD32F101xC/D/E/F/G//K devices)

| Symbol | Parameter | Conditions | Min | Typ. | Max | Unit |
|-----------------|-------------------------------------------------------------------|----------------------------------|----------------------|------|----------------------|------|
| V _{IL} | Standard IO Low level input voltage | 2.6V ≤ V _{DD} ≤ 3.6V | -0.3 | — | 0.8 | V |
| | 5V-tolerant IO Low level input voltage | 2.6V ≤ V _{DD} ≤ 3.6V | -0.3 | — | 0.8 | V |
| V _{IH} | Standard IO High level input voltage | 2.6V ≤ V _{DD} ≤ 3.6V | 2 | — | V _{DD} +0.3 | V |
| | 5V-tolerant IO High level input voltage | 2.6V ≤ V _{DD} ≤ 3.6V | 2 | — | 5.5 | V |
| V _{OL} | Output low level voltage for an IO pin (I _{IO} = +8mA) | 2.6V ≤ V _{DD} ≤ 3.6V | — | — | 0.3 | V |
| V _{OH} | Output high level voltage for an IO pin (I _{IO} = +8mA) | 2.6V ≤ V _{DD} ≤ 3.6V | V _{DD} -0.3 | — | — | V |
| V _{OL} | Output low level voltage for an IO pin (I _{IO} = +20mA) | 2.6V ≤ V _{DD} ≤ 3.6V | — | — | 0.7 | V |
| V _{OH} | Output high level voltage for an IO pin (I _{IO} = +20mA) | 2.6V ≤ V _{DD} ≤ 3.6V | V _{DD} -0.8 | — | — | V |
| R _{PU} | Internal pull-up resistor | V _{IN} =V _{SS} | 30 | 40 | 50 | kΩ |
| R _{PD} | Internal pull-down resistor | V _{IN} =V _{DD} | 30 | 40 | 50 | kΩ |

4.12. ADC characteristics

Table 4-19. ADC characteristics

| Symbol | Parameter | Conditions | Min | Typ. | Max | Unit |
|----------------------|----------------------------------|---------------------------------|-----|------|-------------------|------|
| V _{DDA} | Operating voltage | | 2.6 | 3.3 | 3.6 | V |
| V _{IN} | ADC input voltage range | | 0 | — | V _{REF+} | V |
| f _{ADC} | ADC clock | | 0.6 | — | 14 | MHz |
| f _s | Sampling rate | | — | — | 1 | MHz |
| f _{ADCCONV} | ADC conversion time | f _{ADC} =14MHz | 1 | — | 18 | μs |
| R _{ADC} | Input sampling switch resistance | | — | — | 0.2 | kΩ |
| C _{ADC} | Input sampling capacitance | No pin/pad capacitance included | — | 32 | — | pF |
| t _{SU} | Startup time | | — | — | 1 | μs |

4.13. I2C characteristics

Table 4-20. I2C characteristics

| Symbol | Parameter | Conditions | Standard mode | | Fast mode | | Unit |
|---------------------|---------------------|------------|---------------|-----|-----------|-----|------|
| | | | Min | Max | Min | Max | |
| f _{SCL} | SCL clock frequency | | 0 | 100 | 0 | 400 | KHz |
| t _{SCL(H)} | SCL clock high time | | 4.0 | — | 0.6 | — | ns |
| t _{SCL(L)} | SCL clock low time | | 4.7 | — | 1.3 | — | ns |

4.14. SPI characteristics

Table 4-21. Standard SPI characteristics

| Symbol | Parameter | Conditions | Min | Typ. | Max | Unit |
|------------------------|-------------------------|--------------------------|-----|------|-----|------|
| f _{SCK} | SCK clock frequency | | — | — | 18 | MHz |
| t _{SCK(H)} | SCK clock high time | | 19 | — | — | ns |
| t _{SCK(L)} | SCK clock low time | | 19 | — | — | ns |
| SPI master mode | | | | | | |
| t _{V(MO)} | Data output valid time | | — | — | 25 | ns |
| t _{H(MO)} | Data output hold time | | 2 | — | — | ns |
| t _{SU(MI)} | Data input setup time | | 5 | — | — | ns |
| t _{H(MI)} | Data input hold time | | 5 | — | — | ns |
| SPI slave mode | | | | | | |
| t _{SU(NSS)} | NSS enable setup time | f _{PCLK} =54MHz | 74 | — | — | ns |
| t _{H(NSS)} | NSS enable hold time | f _{PCLK} =54MHz | 37 | — | — | ns |
| t _{A(SO)} | Data output access time | f _{PCLK} =54MHz | 0 | — | 55 | ns |

| | | | | | | |
|---------------|--------------------------|--|----|---|----|----|
| $t_{DIS(SO)}$ | Data output disable time | | 3 | — | 10 | ns |
| $t_{V(SO)}$ | Data output valid time | | — | — | 25 | ns |
| $t_{H(SO)}$ | Data output hold time | | 15 | — | — | ns |
| $t_{SU(SI)}$ | Data input setup time | | 5 | — | — | ns |
| $t_{H(SI)}$ | Data input hold time | | 4 | — | — | ns |

5. Package information

5.1. QFN package outline dimensions

Figure 5-1. QFN package outline

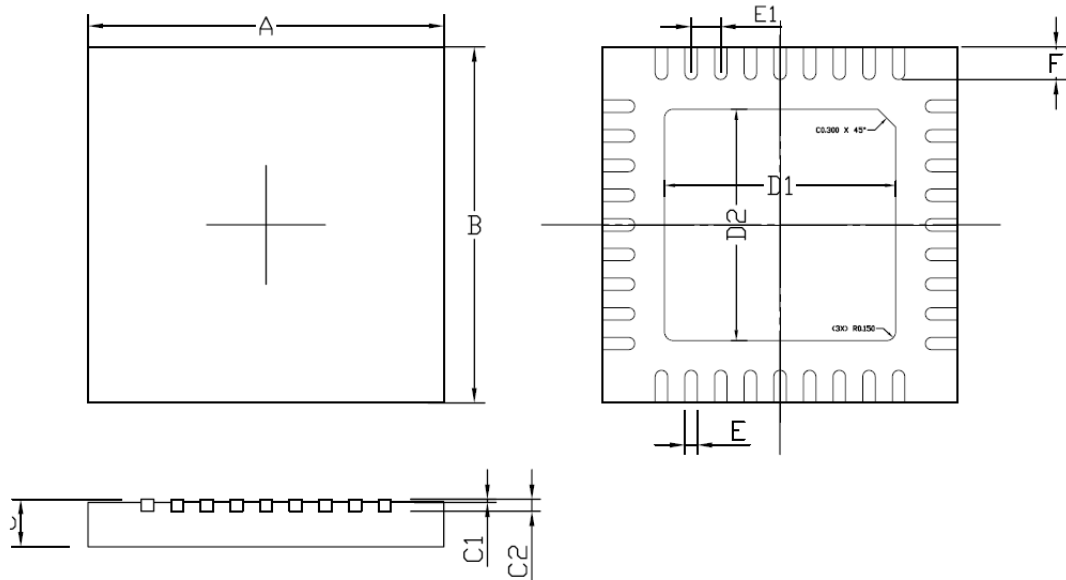


Table 5-1. QFN package dimensions

| Symbol | Dimensions (mm) | | Symbol | Dimensions (mm) | |
|--------|-----------------|------|--------|-----------------|-----|
| | min | max | | min | max |
| A | 6.0 ± 0.1 | | D1 | 3.90 Typ. | |
| B | 6.0 ± 0.1 | | D2 | 3.90 Typ. | |
| C | 0.85 | 0.95 | E | 0.210 ± 0.025 | |
| C1 | 0~0.050 | | E1 | 0.500 Typ. | |
| C2 | 0.203 Typ. | | F | 0.550 Typ. | |

Notes:

1. Formed lead shall be planar with respect to one another within 0.004 inches.
2. Both package length and width do not include mold flash and metal burr.

5.2. LQFP package outline dimensions

Figure 5-2. LQFP package outline

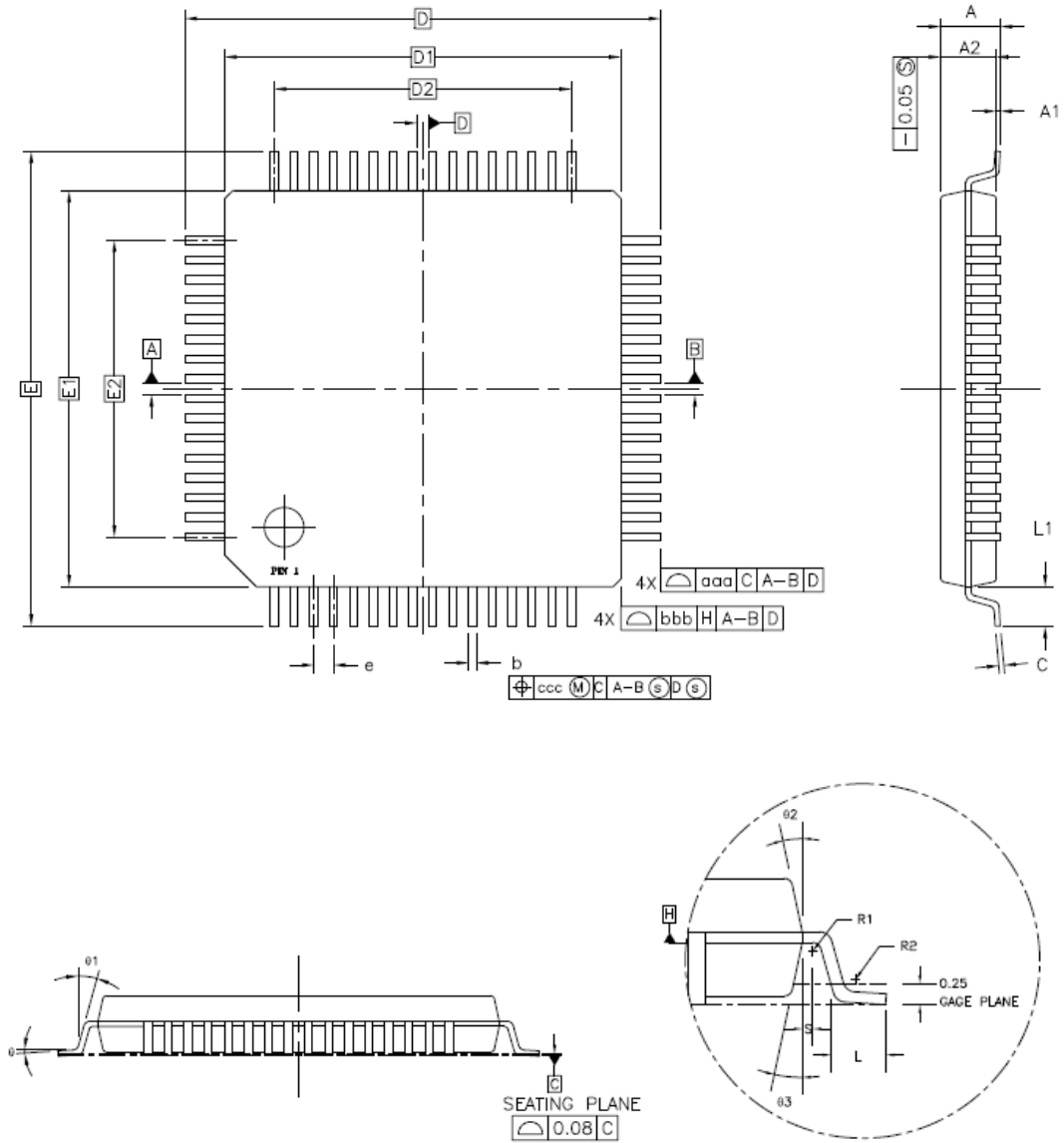


Table 5-2. LQFP package dimensions

| Symbol | LQFP48 | | | LQFP64 | | | LQFP100 | | | LQFP144 | | |
|--------|--------|------|------|--------|-------|------|---------|-------|------|---------|-------|------|
| | Min | Typ. | Max | Min | Typ. | Max | Min | Typ. | Max | Min | Typ. | Max |
| A | - | - | 1.20 | - | - | 1.60 | - | - | 1.60 | - | - | 1.60 |
| A1 | 0.05 | - | 0.15 | 0.05 | - | 0.15 | 0.05 | - | 0.15 | 0.05 | - | 0.15 |
| A2 | 0.95 | 1.00 | 1.05 | 1.35 | 1.40 | 1.45 | 1.35 | 1.40 | 1.45 | 1.35 | 1.40 | 1.45 |
| D | - | 9.00 | - | - | 12.00 | - | - | 16.00 | - | - | 22.00 | - |
| D1 | - | 7.00 | - | - | 10.00 | - | - | 14.00 | - | - | 20.00 | - |
| E | - | 9.00 | - | - | 12.00 | - | - | 16.00 | - | - | 22.00 | - |
| E1 | - | 7.00 | - | - | 10.00 | - | - | 14.00 | - | - | 20.00 | - |
| R1 | 0.08 | - | - | 0.08 | - | - | 0.08 | - | - | 0.08 | - | - |
| R2 | 0.08 | - | 0.20 | 0.08 | - | 0.20 | 0.08 | - | 0.20 | 0.08 | - | 0.20 |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| θ1 | 0° | - | - | 0° | - | - | 0° | - | - | 0° | - | - |
| θ2 | 11° | 12° | 13° | 11° | 12° | 13° | 11° | 12° | 13° | 11° | 12° | 13° |
| θ3 | 11° | 12° | 13° | 11° | 12° | 13° | 11° | 12° | 13° | 11° | 12° | 13° |
| c | 0.09 | - | 0.20 | 0.09 | - | 0.20 | 0.09 | - | 0.20 | 0.09 | - | 0.20 |
| L | 0.45 | 0.60 | 0.75 | 0.45 | 0.60 | 0.75 | 0.45 | 0.60 | 0.75 | 0.45 | 0.60 | 0.75 |
| L1 | - | 1.00 | - | - | 1.00 | - | - | 1.00 | - | - | 1.00 | - |
| S | 0.20 | - | - | 0.20 | - | - | 0.20 | - | - | 0.20 | - | - |
| b | 0.17 | 0.22 | 0.27 | 0.17 | 0.20 | 0.27 | 0.17 | 0.20 | 0.27 | 0.17 | 0.20 | 0.27 |
| e | - | 0.50 | - | - | 0.50 | - | - | 0.50 | - | - | 0.50 | - |
| D2 | - | 5.50 | - | - | 7.50 | - | - | 12.00 | - | - | 17.50 | - |
| E2 | - | 5.50 | - | - | 7.50 | - | - | 12.00 | - | - | 17.50 | - |
| aaa | 0.20 | | | 0.20 | | | 0.20 | | | 0.20 | | |
| bbb | 0.20 | | | 0.20 | | | 0.20 | | | 0.20 | | |
| ccc | 0.08 | | | 0.08 | | | 0.08 | | | 0.08 | | |

(Original dimensions are in millimeters)

6. Ordering Information

Table 6-1. Part ordering code for GD32F101xx devices

| Ordering code | Flash (KB) | Package | Package type | Temperature operating range |
|---------------|------------|---------|--------------|------------------------------|
| GD32F101T4U6 | 16 | QFN36 | Green | Industrial -40°C to +85°C |
| GD32F101T6U6 | 32 | QFN36 | Green | Industrial -40°C to +85°C |
| GD32F101T8U6 | 64 | QFN36 | Green | Industrial -40°C to +85°C |
| GD32F101TBU6 | 128 | QFN36 | Green | Industrial -40°C to +85°C |
| GD32F101C4T6 | 16 | LQFP48 | Green | Industrial -40°C to +85°C |
| GD32F101C6T6 | 32 | LQFP48 | Green | Industrial -40°C to +85°C |
| GD32F101C8T6 | 64 | LQFP48 | Green | Industrial -40°C to +85°C |
| GD32F101CBT6 | 128 | LQFP48 | Green | Industrial -40°C to +85°C |
| GD32F101R4T6 | 16 | LQFP64 | Green | Industrial -40°C to +85°C |
| GD32F101R6T6 | 32 | LQFP64 | Green | Industrial -40°C to +85°C |
| GD32F101R8T6 | 64 | LQFP64 | Green | Industrial -40°C to +85°C |
| GD32F101RBT6 | 128 | LQFP64 | Green | Industrial -40°C to +85°C |
| GD32F101RCT6 | 256 | LQFP64 | Green | Industrial -40°C to +85°C |
| GD32F101RDT6 | 384 | LQFP64 | Green | Industrial -40°C to +85°C |
| GD32F101RET6 | 512 | LQFP64 | Green | Industrial -40°C to +85°C |
| GD32F101RFT6 | 768 | LQFP64 | Green | Industrial -40°C to +85°C |
| GD32F101RGT6 | 1024 | LQFP64 | Green | Industrial -40°C to +85°C |
| GD32F101RIT6 | 2048 | LQFP64 | Green | Industrial -40°C to +85°C |
| GD32F101RKT6 | 3072 | LQFP64 | Green | Industrial -40°C to +85°C |
| GD32F101V8T6 | 64 | LQFP100 | Green | Industrial -40°C to +85°C |
| GD32F101VBT6 | 128 | LQFP100 | Green | Industrial -40°C to +85°C |
| GD32F101VCT6 | 256 | LQFP100 | Green | Industrial -40°C to +85°C |
| GD32F101VDT6 | 384 | LQFP100 | Green | Industrial -40°C to +85°C |
| GD32F101VET6 | 512 | LQFP100 | Green | Industrial -40°C to +85°C |
| GD32F101VFT6 | 768 | LQFP100 | Green | Industrial |

| Ordering code | Flash (KB) | Package | Package type | Temperature operating range |
|---------------|------------|---------|--------------|------------------------------|
| | | | | -40°C to +85°C |
| GD32F101VGT6 | 1024 | LQFP100 | Green | Industrial -40°C to +85°C |
| GD32F101VIT6 | 2048 | LQFP100 | Green | Industrial -40°C to +85°C |
| GD32F101VKT6 | 3072 | LQFP100 | Green | Industrial -40°C to +85°C |
| GD32F101ZCT6 | 256 | LQFP144 | Green | Industrial -40°C to +85°C |
| GD32F101ZDT6 | 384 | LQFP144 | Green | Industrial -40°C to +85°C |
| GD32F101ZET6 | 512 | LQFP144 | Green | Industrial -40°C to +85°C |
| GD32F101ZFT6 | 768 | LQFP144 | Green | Industrial -40°C to +85°C |
| GD32F101ZGT6 | 1024 | LQFP144 | Green | Industrial -40°C to +85°C |
| GD32F101ZIT6 | 2048 | LQFP144 | Green | Industrial -40°C to +85°C |
| GD32F101ZKT6 | 3072 | LQFP144 | Green | Industrial -40°C to +85°C |

7. Revision History

Table 7-1. Revision history

| Revision No. | Description | Date |
|--------------|----------------------------------------------------------|--------------|
| 1.0 | Initial Release | Jun.2, 2013 |
| 2.0 | Characteristics values modified and package data updated | Nov.15, 2013 |
| 2.1 | Characteristics values modified | Aug.18, 2014 |
| 2.2 | Repair history accumulation error | Jan.24, 2018 |