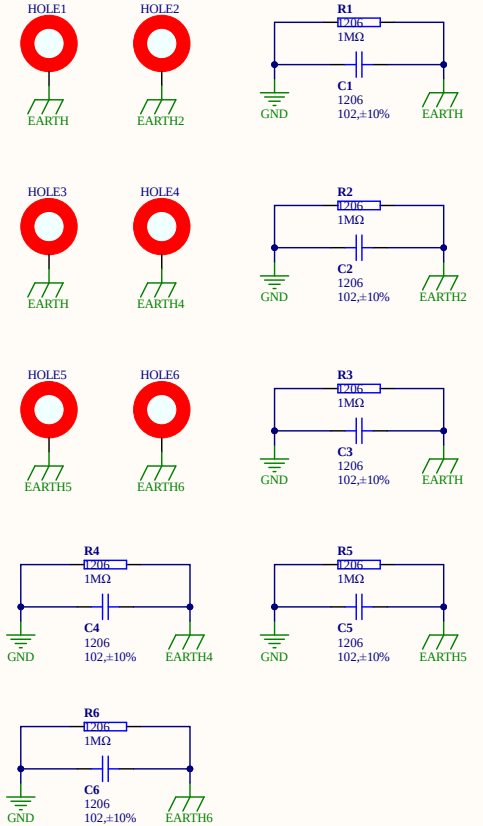
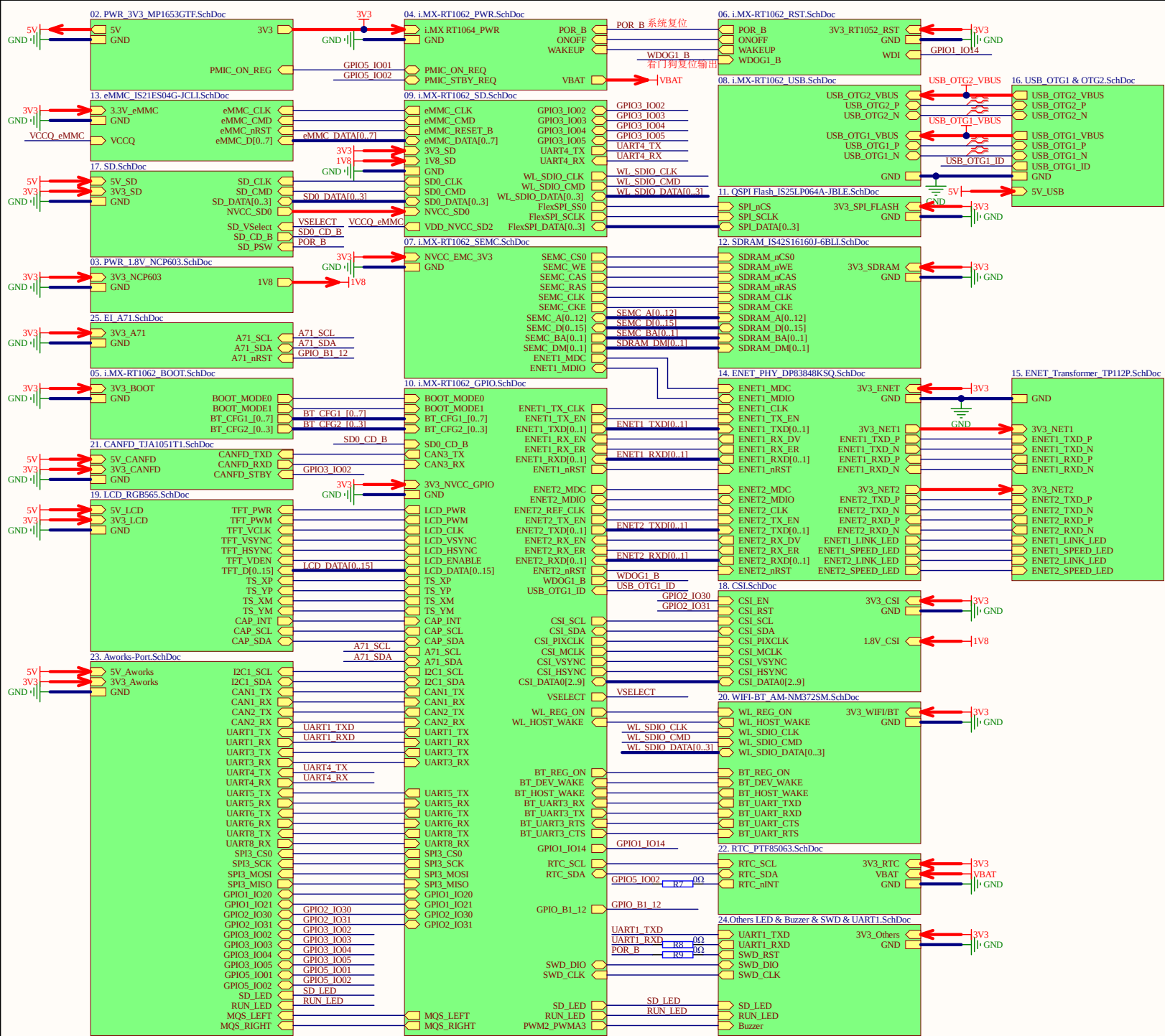


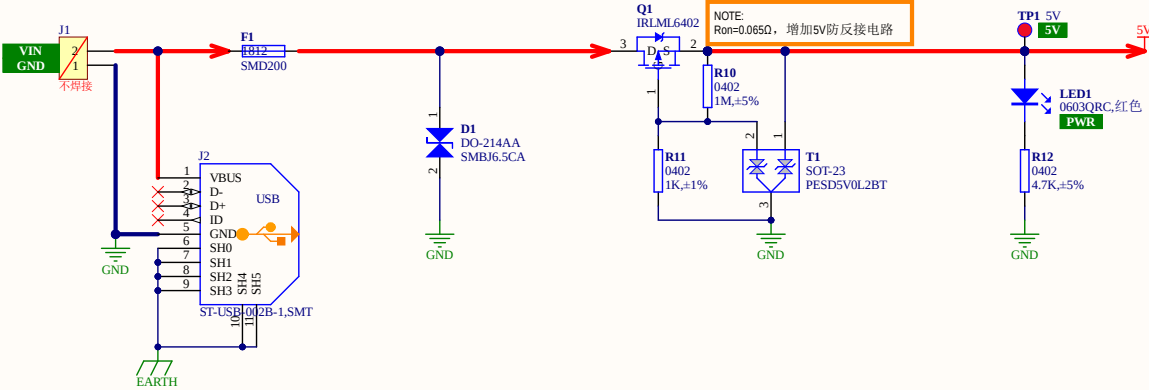
1.MAIN



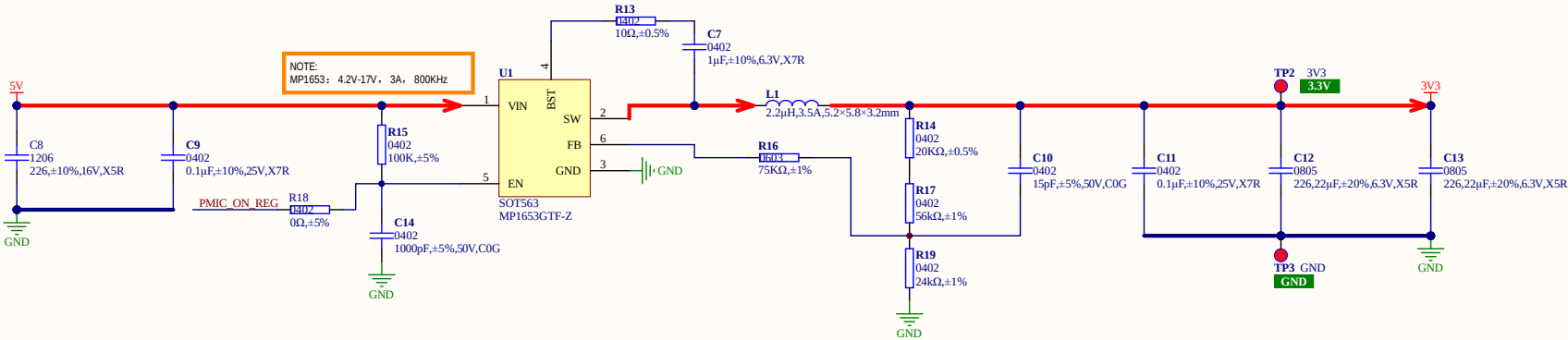
#	修改日期	修改内容
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(2-1) 5V



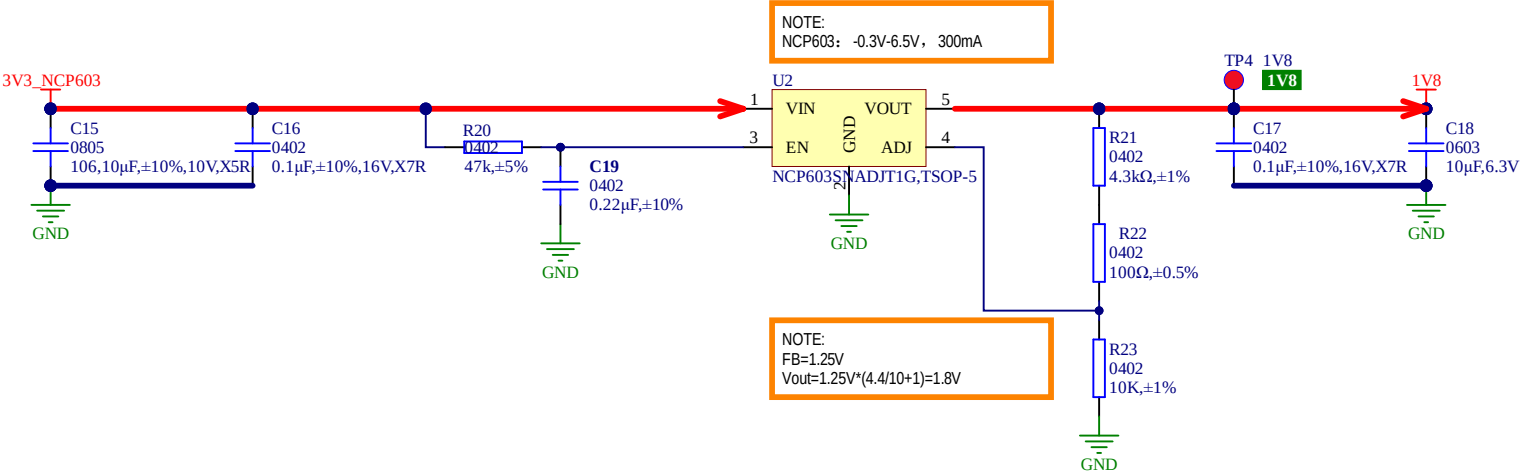
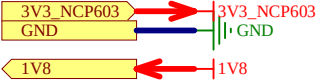
(2-2) 3V3



#	修改日期	修改内容
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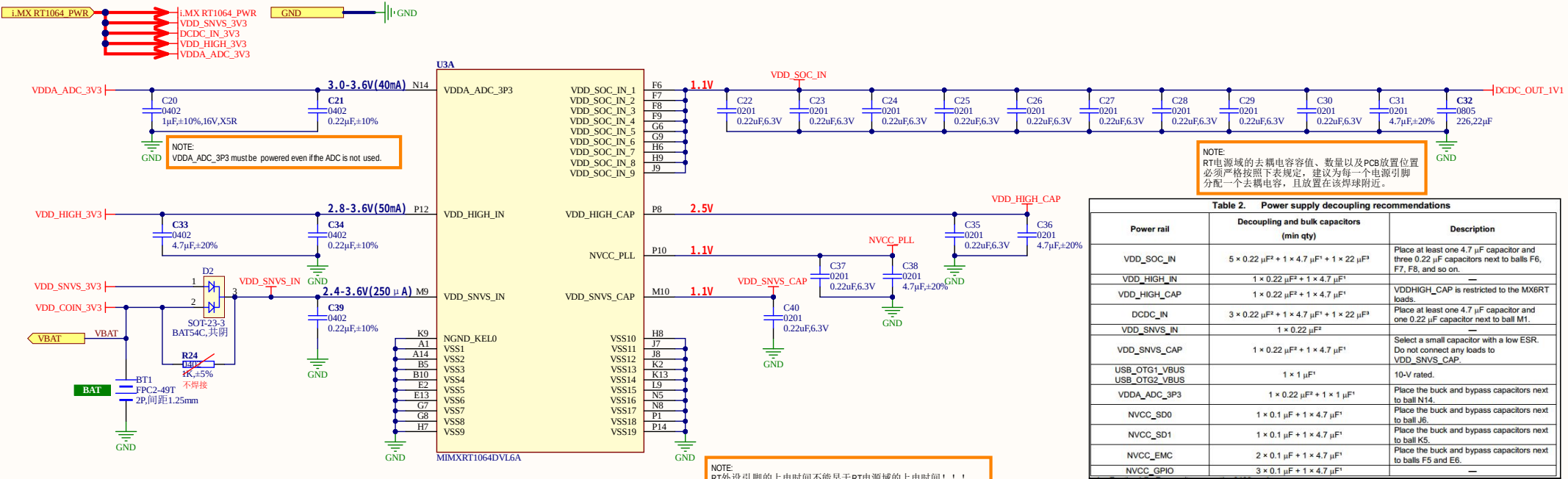
3.PWR_1.8V_NCP603

(3-1) 1V8

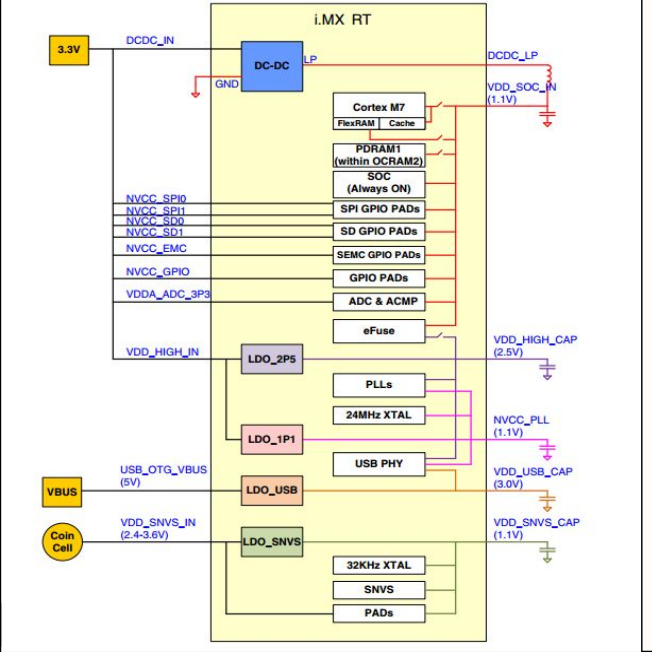
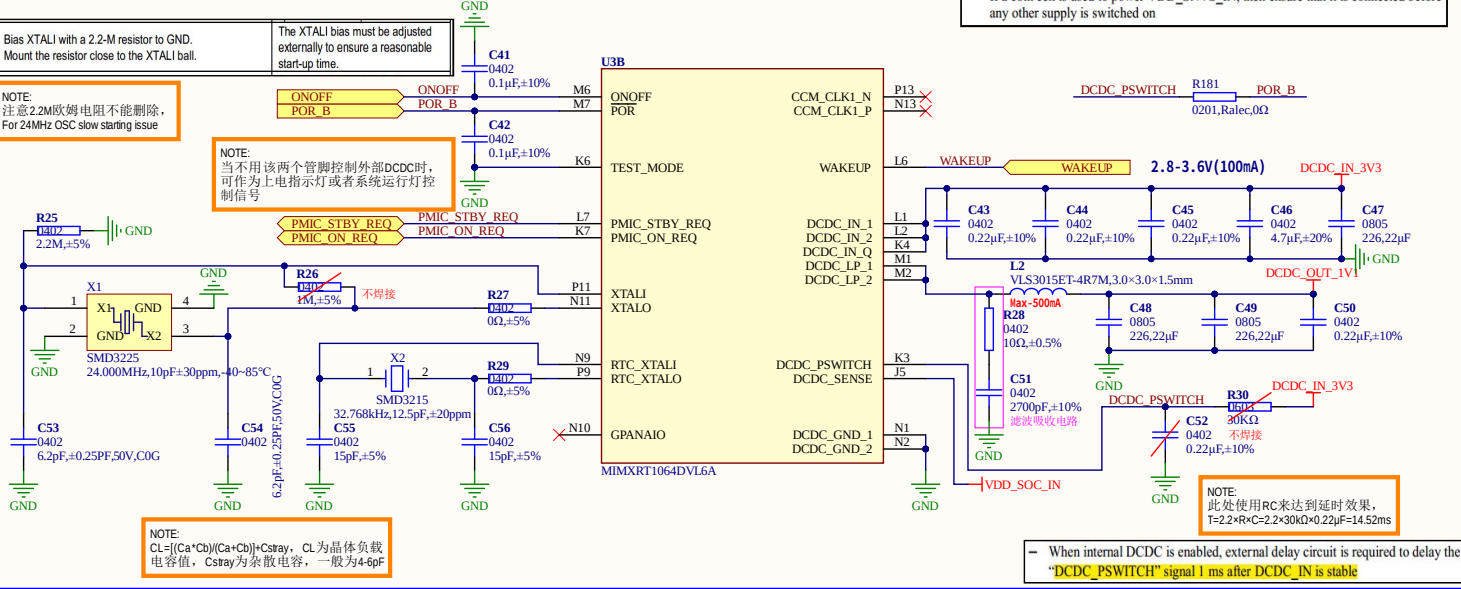


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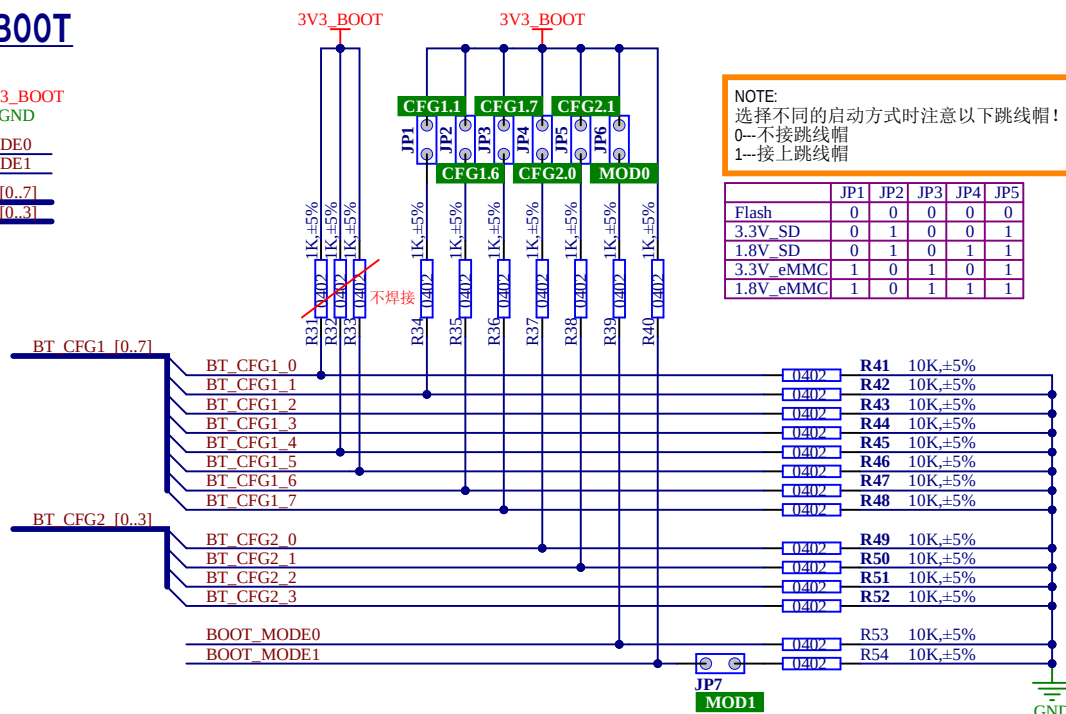
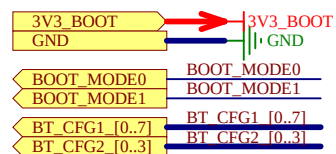
4.i.MX-RT1064_PWR



(4-1) i.MX-RT1064 PWR & CLK



(5-1) RT1064 B00T



NOTE:
选择不同的启动方式时注意以下跳线帽!
0---不接跳线帽
1---接上跳线帽

	JP1	JP2	JP3	JP4	JP5
Flash	0	0	0	0	0
3.3V_SD	0	1	0	0	1
1.8V_SD	0	1	0	1	1
3.3V_eMMC	1	0	1	0	1
1.8V_eMMC	1	0	1	1	1

BOOT_MODE[1:0]	Boot Type
00	Boot From Fuses
01	Serial Downloader
10	Internal Boot 默认状态
11	Reserved

BOOT CFG[17:4]	Boot device
0000b	Serial NOR boot via FlexSPI 默认状态
01xxb	SD Boot via uSDHC
10xxb	eMMC/MMC boot via uSDHC
001xb	SLC NAND boot via SMC
0001b	Parallel NOR boot via SMC
11xxb	Serial NAND boot via FlexSPI

NOTE:

由于BOOT配置信号BT_CFG1、2与LCD信号以及NET2是复用的关系，因此设计中需特别注意。

1、建议仅作为LCD以及NET2输出，当用作其它功能输出时需注意核对外接负载是否改变原本设定的采集电平。

2、建议将该配置信号作为输入使用，如果不得不用，建议采用隔离的方案或者采用模拟开关进行隔离处理。

BOOT TYPE	BT_CFG2_3	BT_CFG2_2	BT_CFG2_1	BT_CFG2_0	BT_CFG1_7	BT_CFG1_6	BT_CFG1_5	BT_CFG1_4	BT_CFG1_3	BT_CFG1_2	BT_CFG1_1	BT_CFG1_0
FlexSPI1 Serial NOR	Loop 0-DIS 1-EN	FLASH TYPE 000-3Byte 001-4Byte 100-MXIC	101-Micron 010-1V8 011-3V3 101-3B secondary	Octal DDR HyperFlash HyperFlash	0	0	0	0	HOLD TIME 00-500us 10-3ms	01-1ms 11-10ms	Encrypted XIP 0-DIS 1-EN	Reserved
SD	Loop 0-DIS 1-EN	Reserved	Bus Width 0-1bit 1-4bit	SD1 Voltage 0-3.3V 1-1.8V	0	1	SD/SDXC Speed 00-N/SDR12 10-SDR50	01-H/SDR25 11-SDR104	SD Cy EN 0-DIS 1-EN	SD CLK SLE 0-SD 1-direct	Port Select 0-eSDHC1 1-eSDHC2	Fast Boot 0-Regular 1-Fast BT
MMC/eMMC	Loop 0-DIS 1-EN	Bus Width: 00-4bit 10-4bit 11-8bit	01-8bit DDR(MMC 4.4) DDR(MMC 4.4)	SD1 Voltage 0-3.3V 1-1.8V	1	0	Speed 0-Normal 1-High	Fast Boot 0-DIS 1-EN	SD Cy EN 0-DIS 1-EN	SD CLK SLE 0-SD 1-direct	Port Select 0-eSDHC1 1-eSDHC2	Fast Boot 0-Regular 1-Fast BT

板载外设

3. BOOT_CFG and BOOT_MODE signals multiplexed with LCD signals

To reduce incorrect boot-up mode selections, do one of the following:

- Use the LCD boot interface lines **only** as processes or **outputs**. Make sure that the LCD boot interface lines are not loaded down (such that the level is interpreted as low during the powerup) when the intent is to be at a high level, or the other way round.
- If the LCD boot signal must be configured as an **input**, isolate the LCD signal from the target driving source with an analog switch and apply the logic value with a second analog switch. Alternately, the peripheral devices with 3-state outputs may be used. Ensure that the output is high-impedance.

Using the LCD boot interface lines as inputs may result in a wrong boot because of the source overvoting the pull resistor value.

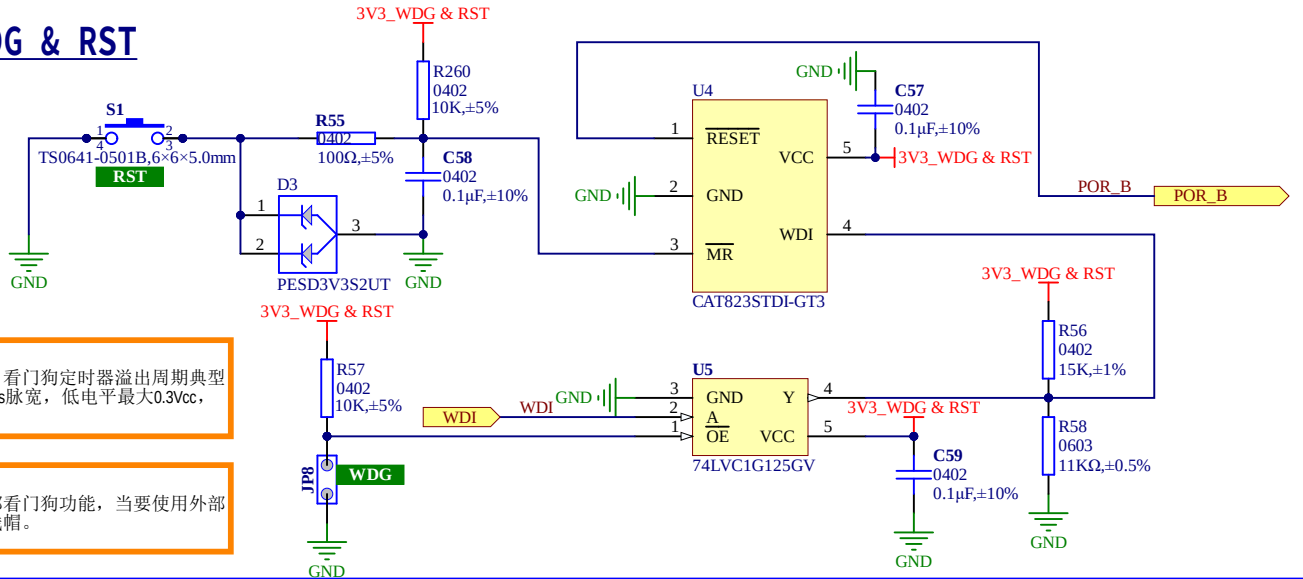
A peripheral device may require the LCD signal to have an external or on-chip resistor to minimize signal floating. If the usage of the LC boot signal affects the peripheral device, then an analog switch, an open collector buffer, or an equivalent shall isolate the path. A pull-up or pull-down resistor at the peripheral device may be required to maintain the desired logic level. See the switch or device data sheet for the operating specifications.

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6.i.MX-RT1064_RST



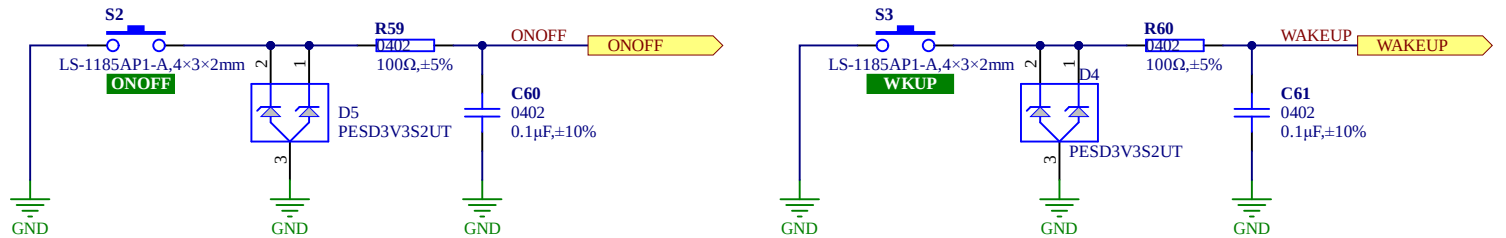
(6-1) RT1064 WDG & RST



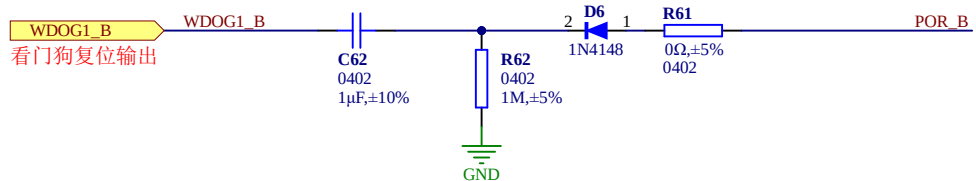
NOTE:
看门狗喂狗信号输入，看门狗定时器溢出周期典型1.6s；喂狗脉冲最小50ns脉宽，低电平最大0.3Vcc，高电平最低0.7Vcc

NOTE:
评估板默认不使用外部看门狗功能，当要使用外部
开门狗功能时接上跳线帽。

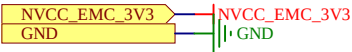
(6-2) RT1064 FUN_Button



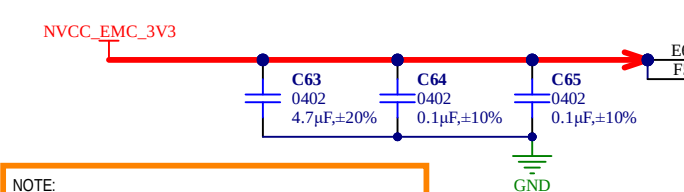
(6-3) SYS_WDG_RST



#	修改日期	修改内容
1		
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(7-1) i.MX-RT1064 SEMC



NOTE:
SEMC支持8/16位SDRAM接口，每个片选支持高达512Mb=64MB，最大支持4个片选

- SDRAM interface
 - Support 8/16 bit modes
 - Up to 512Mb per each Chip Select (CS) and up to 4 CS

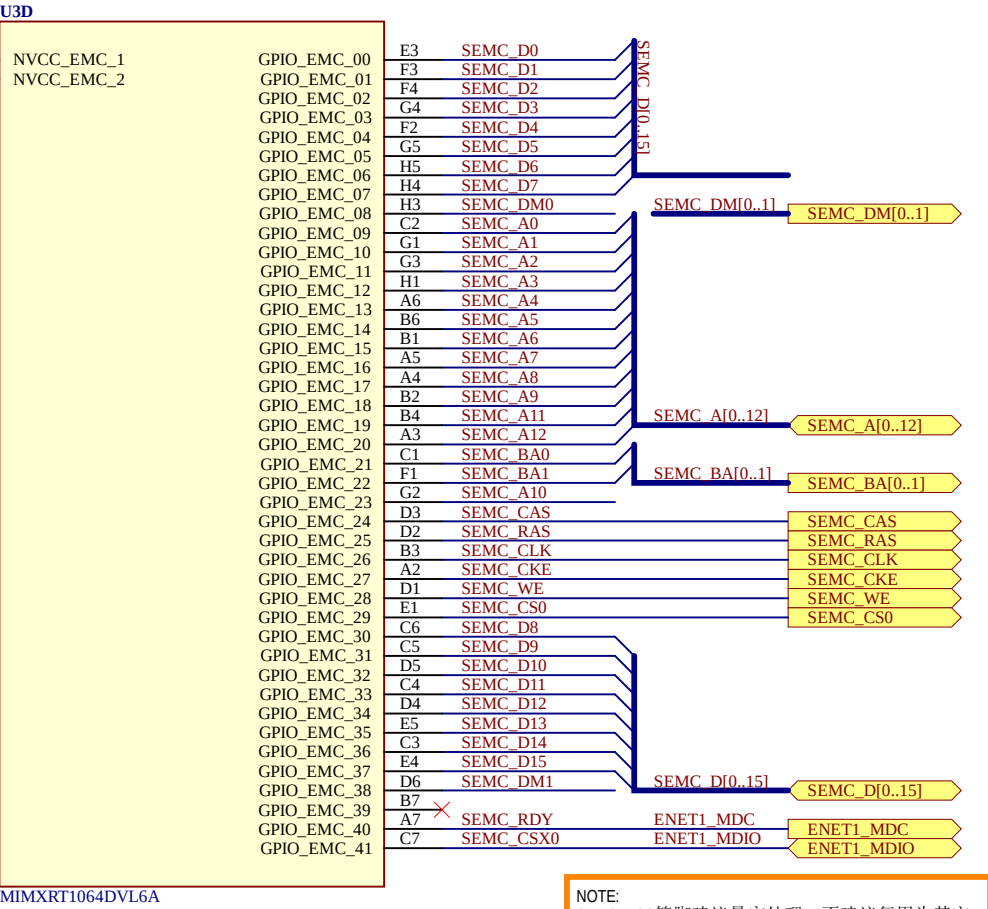
NOTE:
RT105x系列的列地址最小只支持9bit，RT106x系列的列地址最小只支持8bit。因此SDRAM容量选型需注意匹配COL地址位数，避免选型错误：

9-8 COL	Column address bit number 00b - 12 bit 01b - 11 bit 10b - 10 bit 11b - 9 bit	i.MX RT105x系列
7 —	Reserved.	

9-8 COL	Column address bit number 00b - 12 bit 01b - 11 bit 10b - 10 bit 11b - 9 bit	i.MX RT106x系列
7 COL8	Column 8 selection bit 0b - Column address bit number is decided by COL field. 1b - Column address bit number is 8. COL field is ignored.	

NOTE:
对于RT105x系列，16位模式下的容量最小只支持16MB，8MB及以下容量支持不了。
对于RT106x系列，16位模式下的容量最小只支持8MB，4MB及以下容量支持不了。

ADDRESS TABLE		ISSI 8MB容量的COL为8位
Parameter	4M x 16	
Configuration	1M x 16 x 4 banks	
Refresh Count		
Com./Ind.	4K/64ms	
A1	4K/64ms	
A2	4K/16ms	
Row Addresses	A0-A11	RT105x系列不支持
Column Addresses	A0-A7	RT106x系列支持
Bank Address Pins	BA0, BA1	
Auto Precharge Pins	A10/AP	



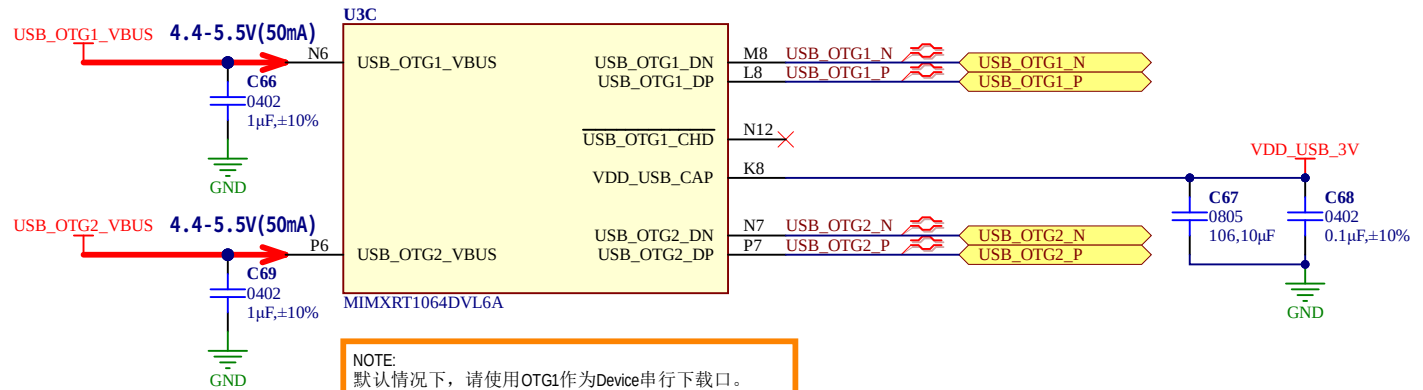
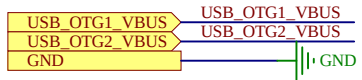
NOTE:
SEMC_DQS管脚建议悬空处理，不建议复用为其它功能。否则SDRAM的时钟只能跑80M，严重的情况甚至会影响SDRAM的使用！

- For the RT1050/RT1060 SEMC module to support SDRAM, SEMC_DQS pin(GPIO_EMC_39) should be kept floating to achieve high-speed access.

#	修改日期	修改内容
1		
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8.i.MX-RT1064_USB

(8-1) USB_OTG1 & HOST2



NOTE:
默认情况下, 请使用OTG1作为Device串行下载口。

NOTE:

- 1、RT支持2路OTG，但不支持同时使用OTG或者device功能。
- 2、详细描述请查阅勘误手册“IMXRT1064CE”中“ERR010661”的描述。
- 3、EasyARM-RT106x将OTG1分为HOST1及DEVICE两个接口，OTG2只做为HOST2。

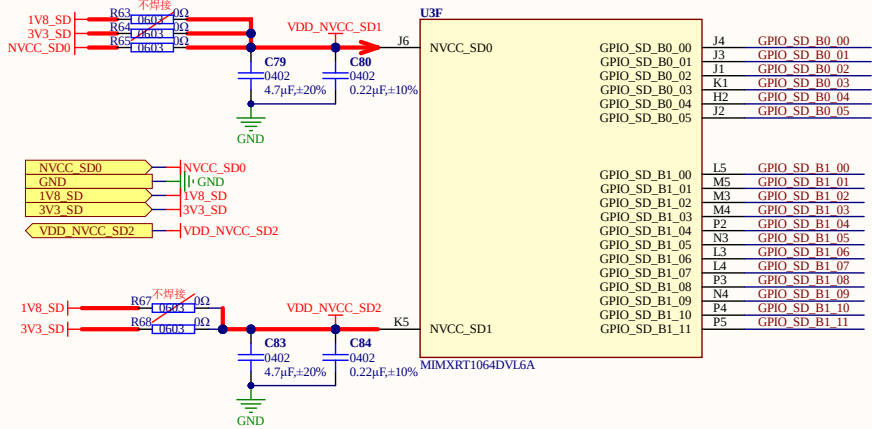
Projected Impact:

Do not use two OTGs or devices simultaneously. Only four scenarios are supported:

- One for OTG/Device, another for Host.
- One for OTG/Device, another is un-used.
- One for Host, another for Host.
- One for Host, another is un-used.

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1		
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(9-1) NVCC_SD



NOTE:
1、多路复用器功能框图如右图所示。
2、多路复用器真值表如右图所示。
3、多路复用器细节参数如下图所示。

- ◆ Single +3.0V to +3.6V Power Supply
- ◆ Low On-Resistance (RON): 8Ω (typ)
- ◆ Low On-Capacitance (CON): 2.5pF (typ)
- ◆ Low Skew: 20ps (typ)
- ◆ 700μA Low Supply Current
- ◆ 2.6GHz (typ) Ultra-High Bandwidth
- ◆ 0.6dB (typ) Ultra-Low Insertion Loss
- ◆ High-Frequency Companion Device to MAX4929

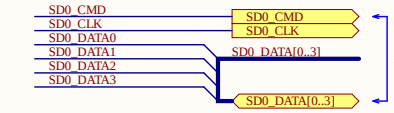
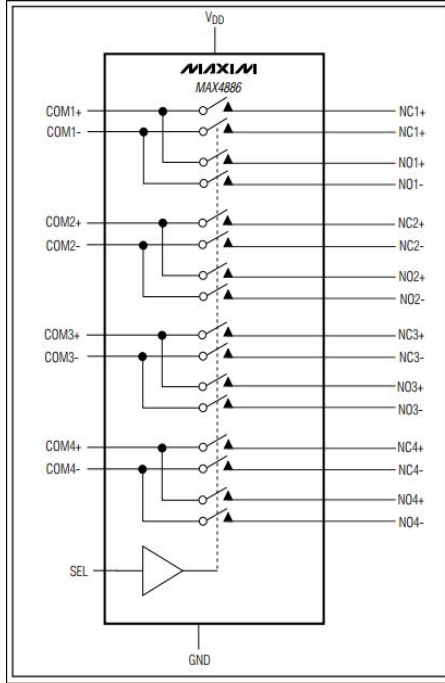
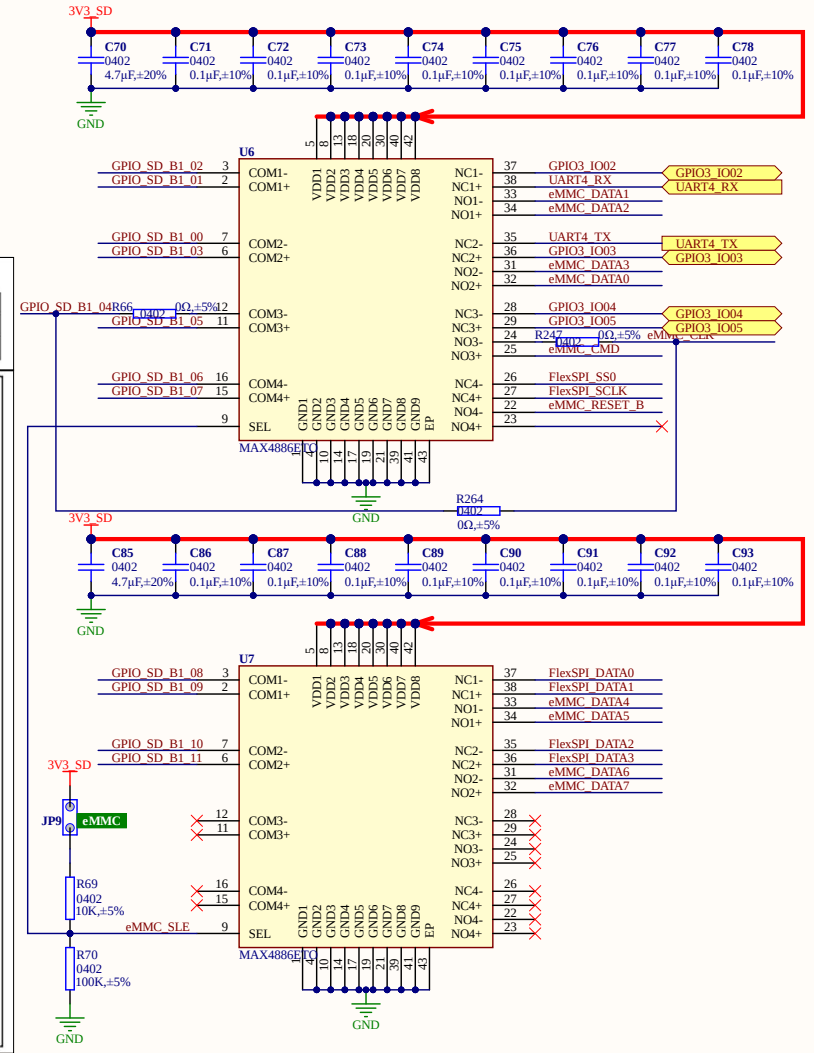
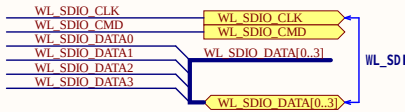


Table 1. Switch Truth Table

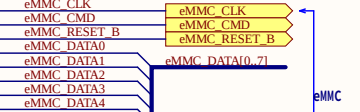
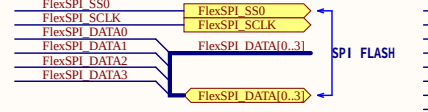
SEL	FUNCTION
0	COM_ to NC_
1	COM_ to NO_



NOTE:
SDIO信号通过数字开关分为两组信号。默认功能为Aworks固定信号(跳线帽不接)。第二功能为外接WIFI-BT模组(跳线帽接上)。二者功能不能同时使用。

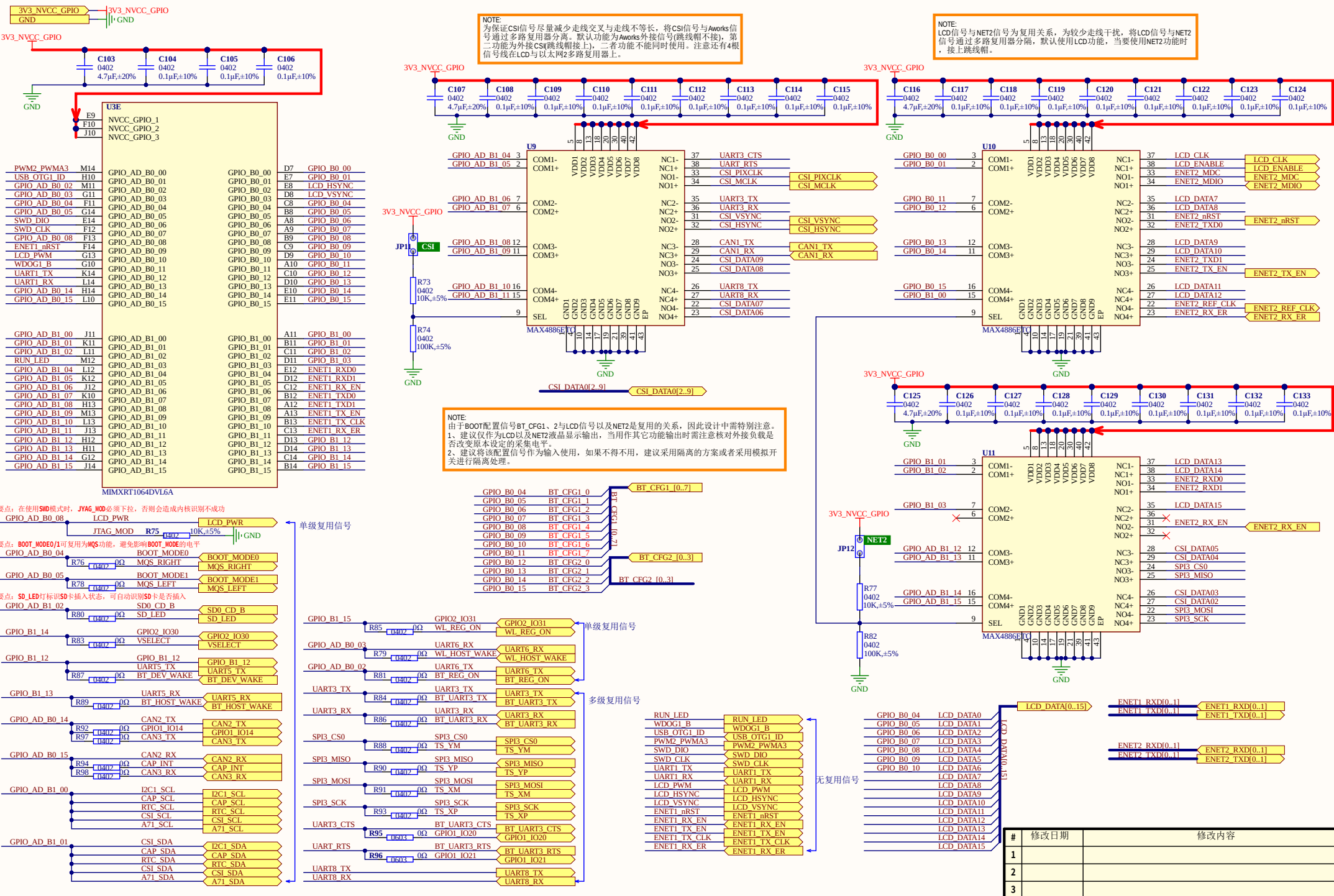


NOTE:
USDHC2信号通过数字开关分为两组信号。默认功能为SDIO与FLEXSPI(跳线帽不接)。第二功能为外接eMMC(跳线帽接上)。二者功能不能同时使用。



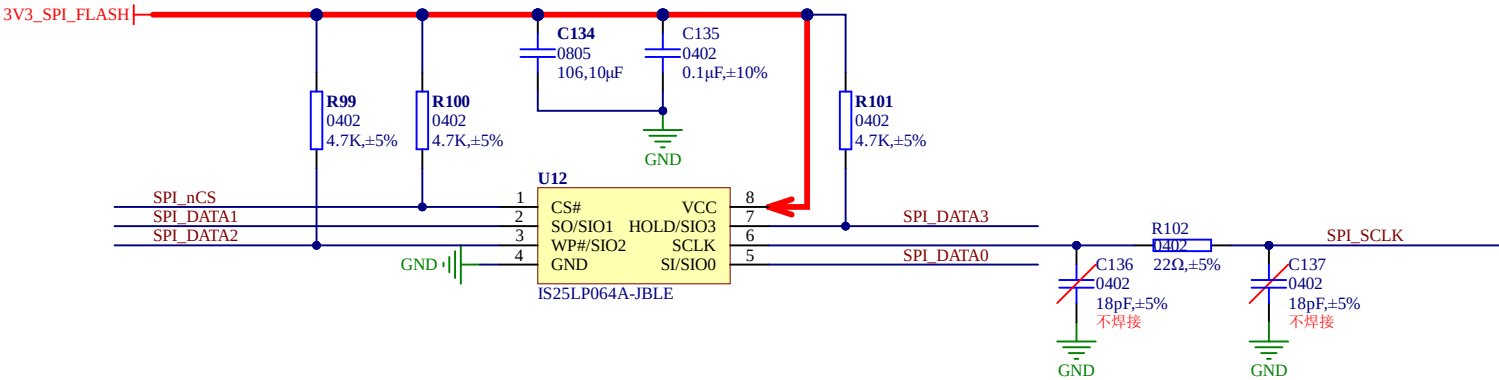
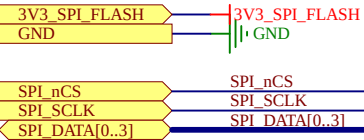
#	修改日期	修改内容
1		
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10.i.MX-RT1064_GPIO



11.QSPI_Flash_IS25LP064A

(11-1) QSPI Flash-8MB



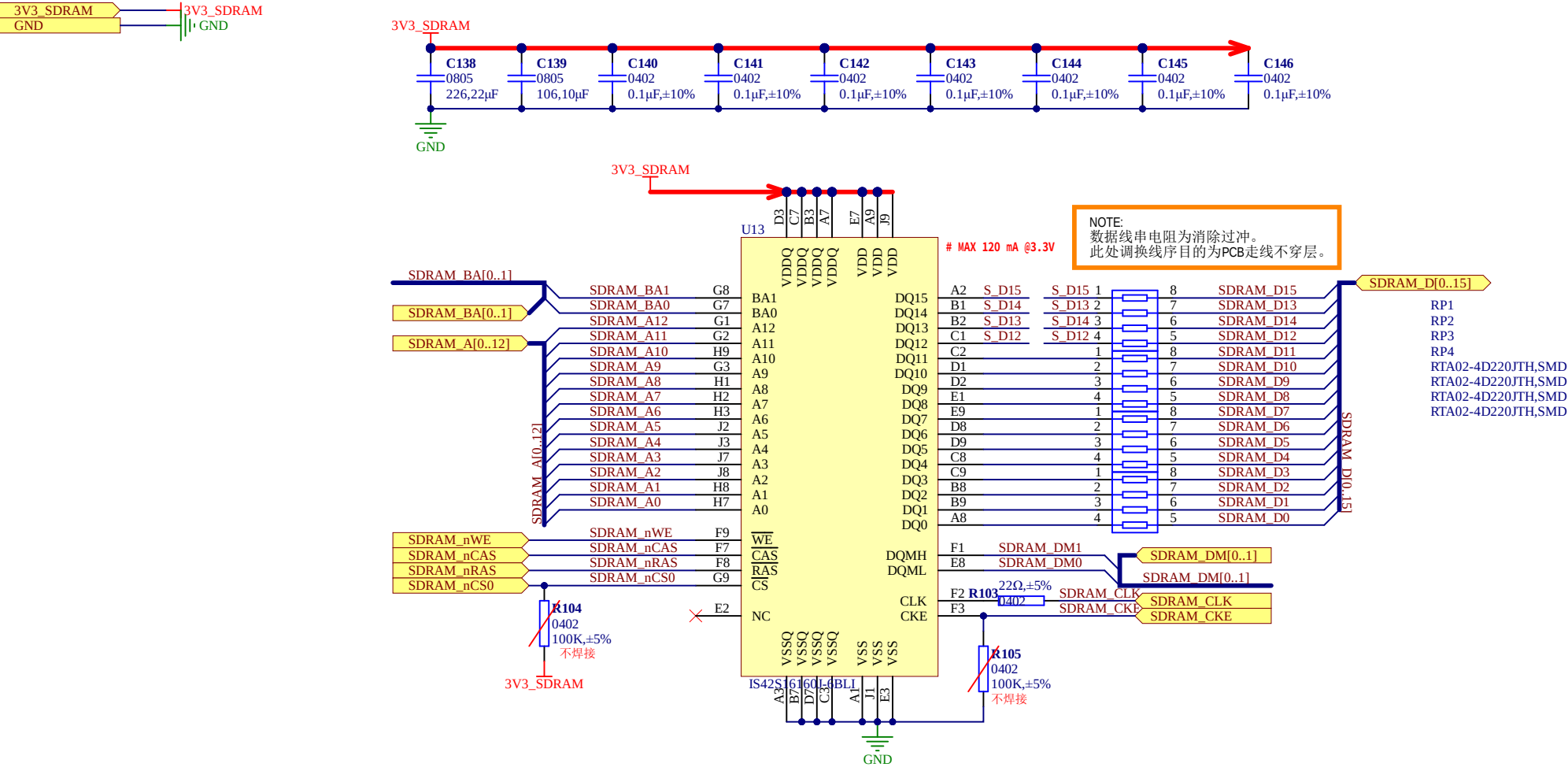
#	修改日期	修改内容
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立功科技

设计人员	<设计人员>	设计日期	2019年8月	图纸名称	QSPI_Flash_IS25LP064A	图纸描述	Flash电路
审核人员	<审核人员>	审核日期	2019年8月	产品名称	评估套件	产品型号	Easy-RT106x
				图纸版本	Rev.A	第 11 张 / 共 25 张	A4

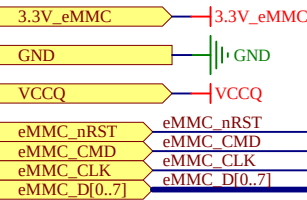
12.SDRAM_IS42S16160J

(12-1) SDRAM-32MB

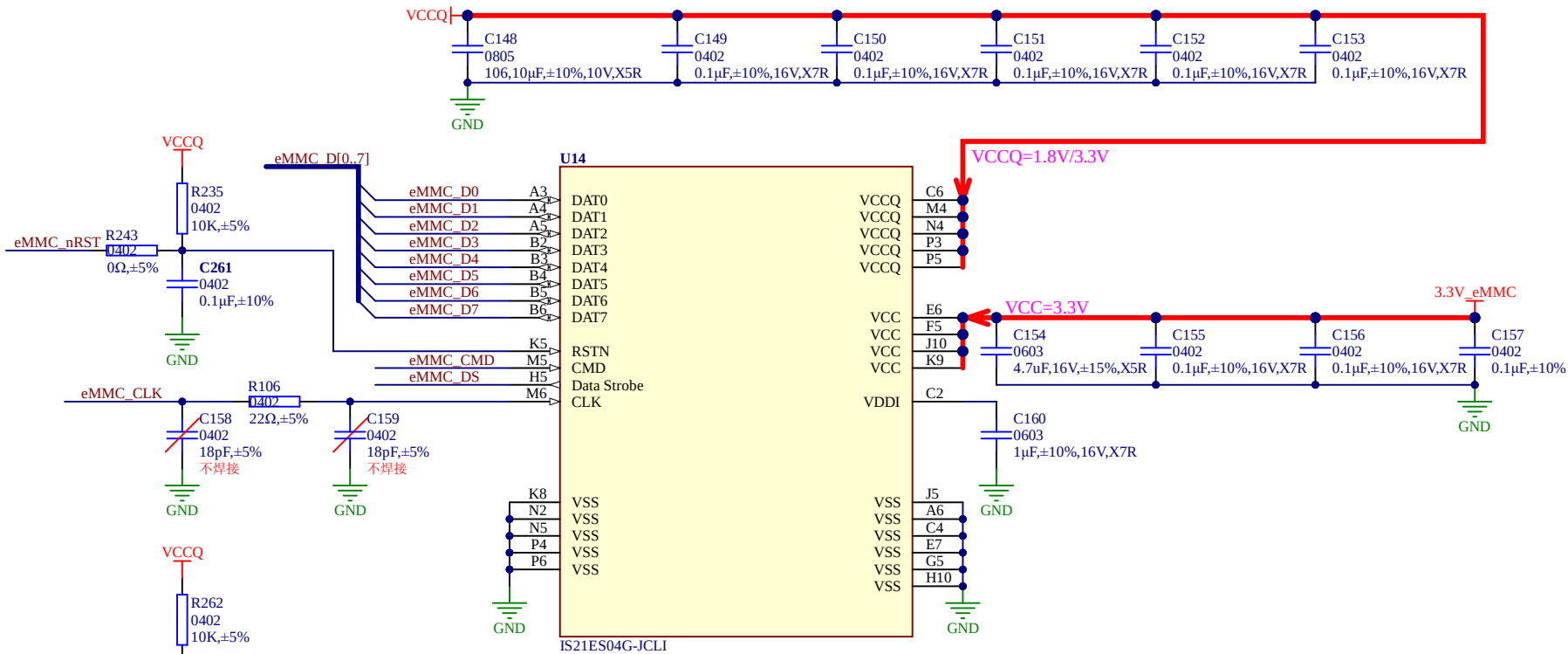


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13.eMMC_IS21ES04G

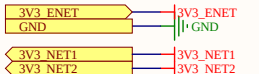


(13-1) eMMC-4GB



#	修改日期	修改内容
1		
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14.ENET_PHY_DP83848KSQ



```
//ENET1配置管理信号
```

ENET1_MDC	ENET1_MDC
ENET1_MDIO	ENET1_MDIO

```
//ENET1时钟[50MHz]
ENET1_CLK
```

```
//ENET1数据发送
ENET1_TX_EN
ENET1_TXD[0..1]
```

//ENET1新掘接收

ENET1_RX_ER	ENET1_RX_ER
ENET1_RX_DV	ENET1_RX_DV
ENET1_RXD[0..1]	ENET1_RXD[0..1]

```
//ENET1复位信号
```

```
//ENET1配置管理信号
```

ENET2_MDC	ENET2_MDC
ENET2_MDIO	ENET2_MDIO

```
//ENET1时钟[50MHz]
ENET2_CLK
```

ENET2_CLK

ENET2_TX_EN	ENET2_TX_EN
ENET2_TXD[0..1]	ENET2_TXD[0..1]

```
//ENET1数据接收
```

ENET2_RX_ER	ENET2_RX_ER
ENET2_RX_DV	ENET2_RX_DV
ENET2_RXD[0..15]	ENET2_RXD[0..15]

ENET2_RXD[0..1]

ENET2_nRST

ENET1 TXD P

ENET1_TXD_P	ENET1_TXD_N
ENET1_TXD_N	ENET1_TXD_P

ENET1_RXD_P	ENET1_RXD_N
ENET1_RXD_N	ENET1_RXD_P

ENET2 TXD P

ENET2_TXD_N

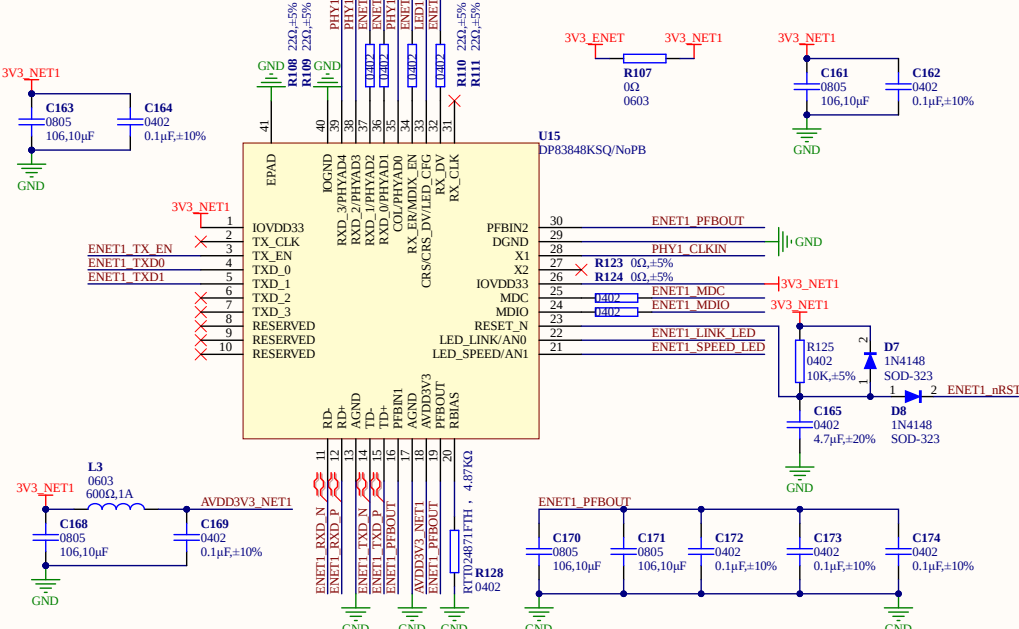
ENET2_RXD_P	ENET2_RXD_P
ENET2_RXD_N	ENET2_RXD_N

ENET1_LINK_LED

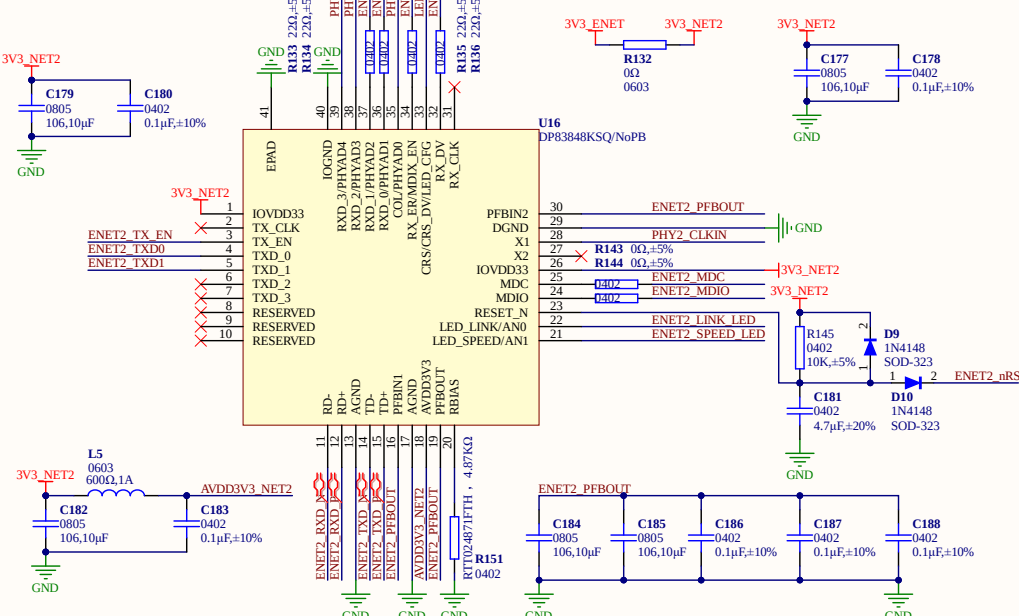
ENET1_SPEED_LED

ENET2_LINK_LED	ENET2_SPEED_LED
ENET2_SPEED_LED	

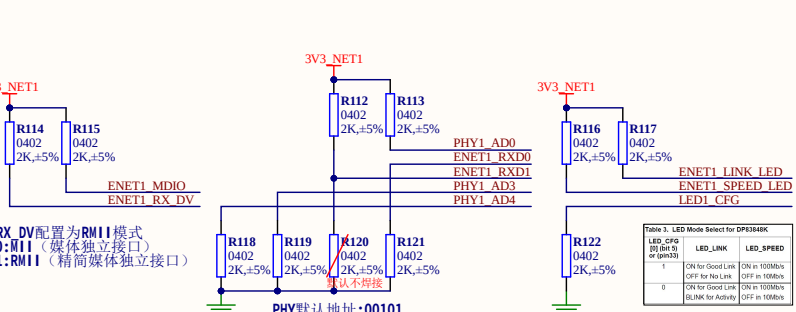
(14-1) ENET1 PHY



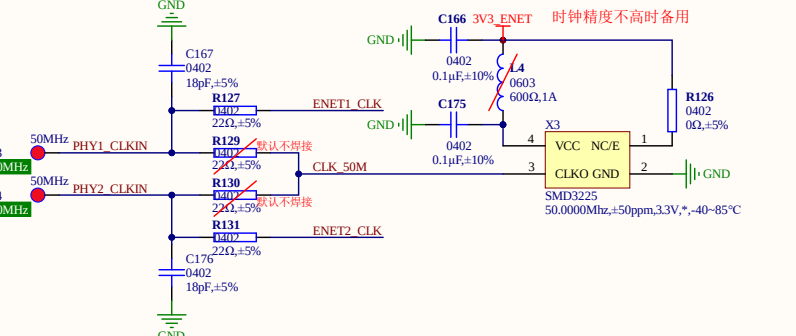
(14-4) ENET2 PHY



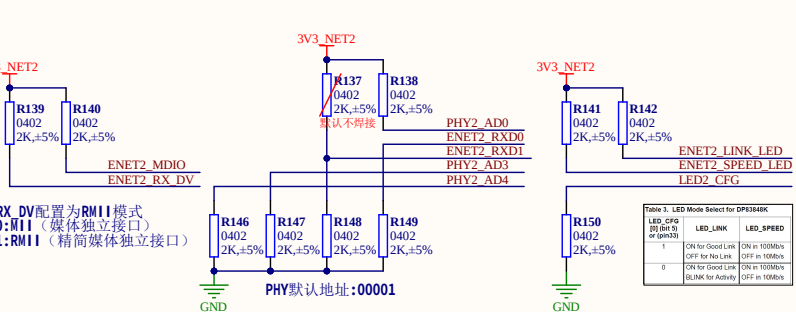
(14-2) PHY1 CFG & ADD



(14-3) PHY CLK

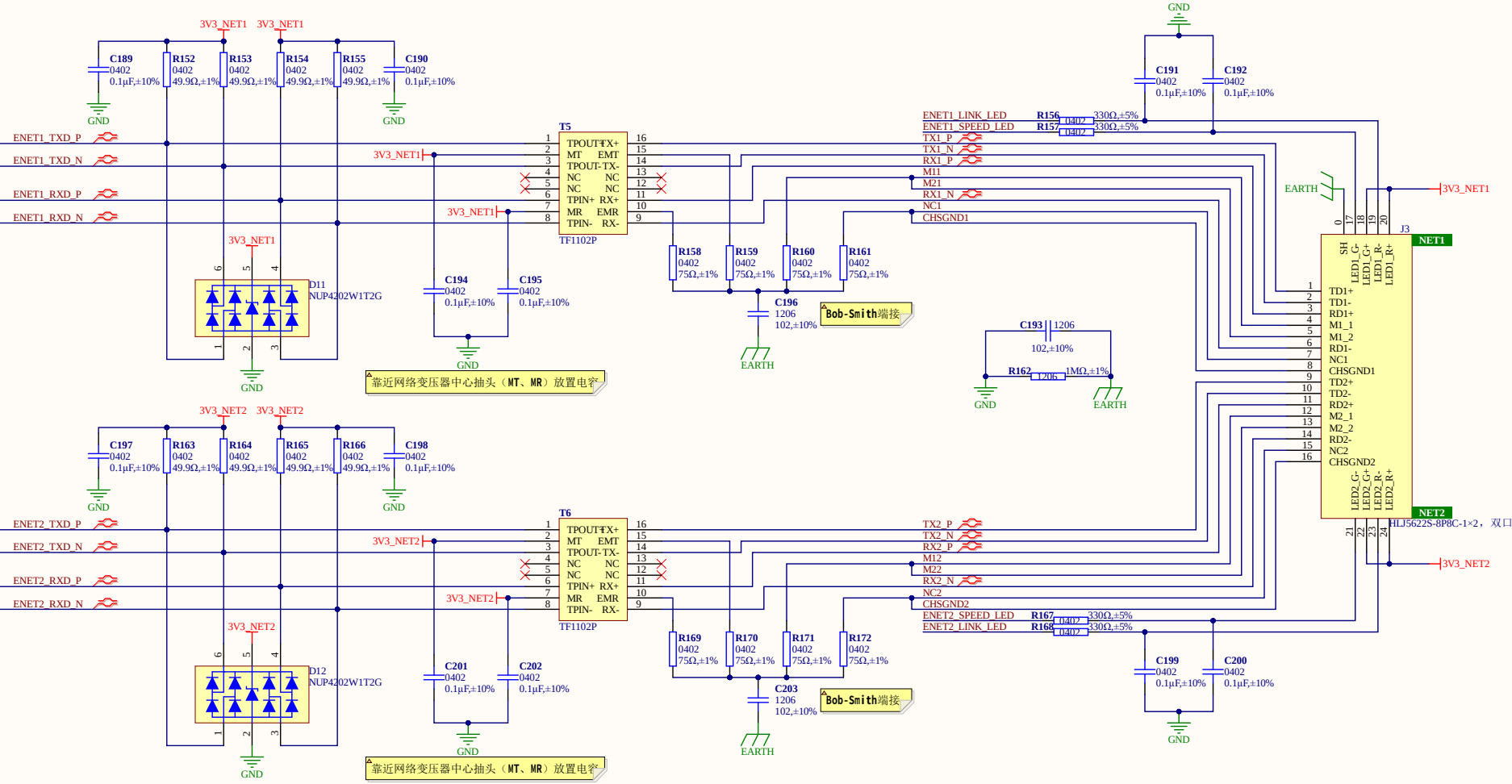
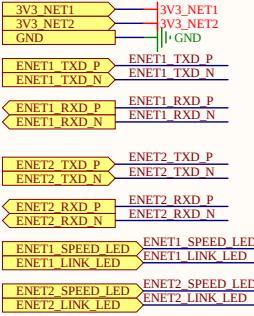


(14-5) PHY2 CFG & ADD



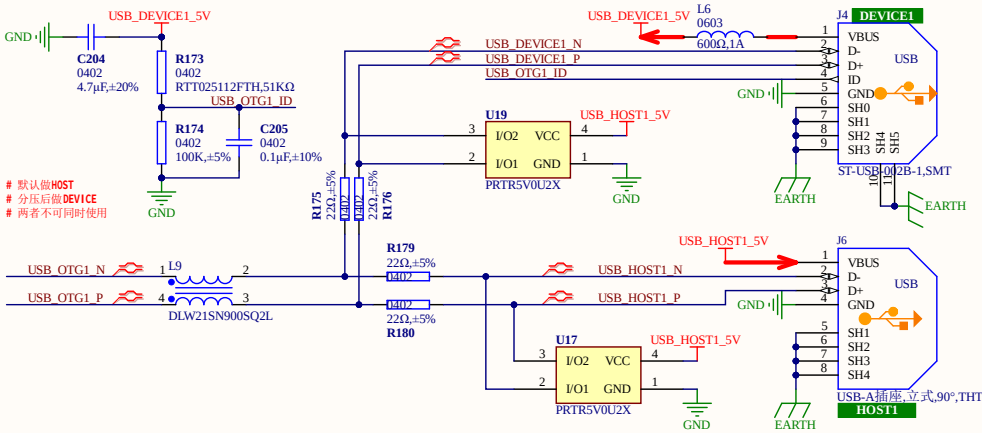
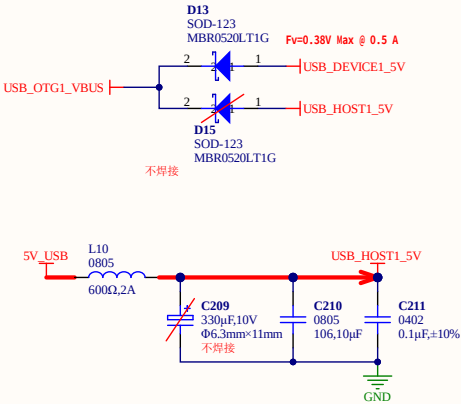
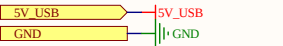
#	修改日期	修改内容
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(15-1) PHY Analog

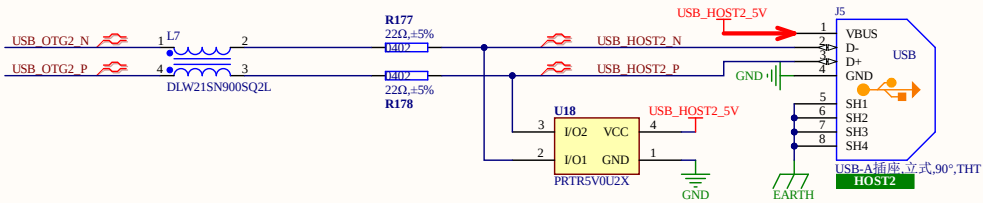
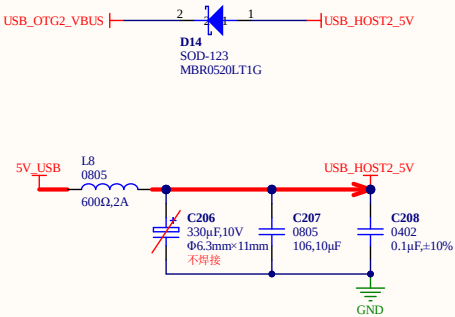
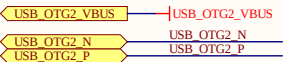


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(16-1) USB_OTG1

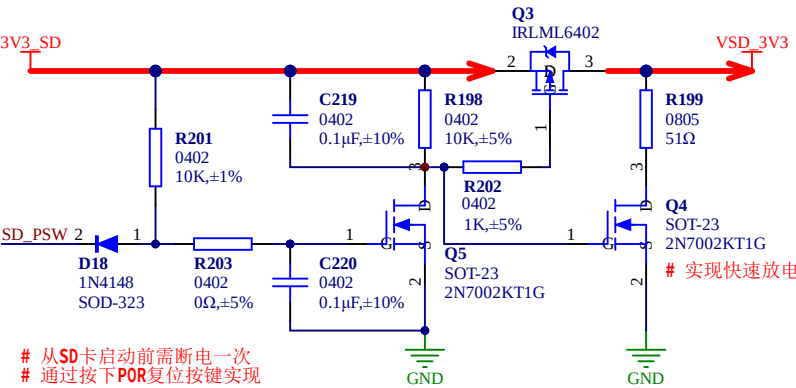
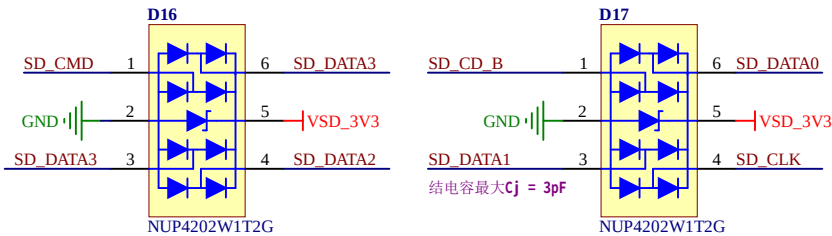
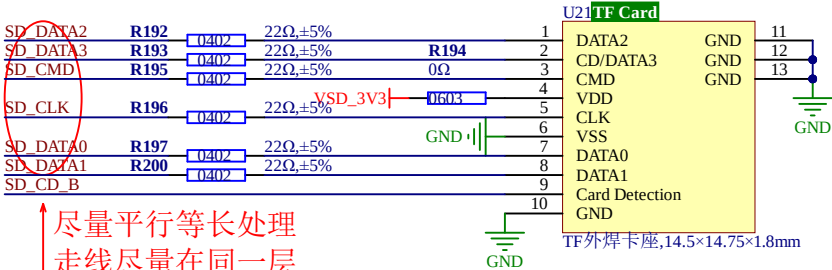
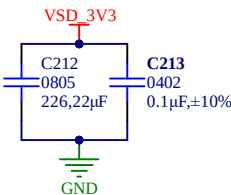
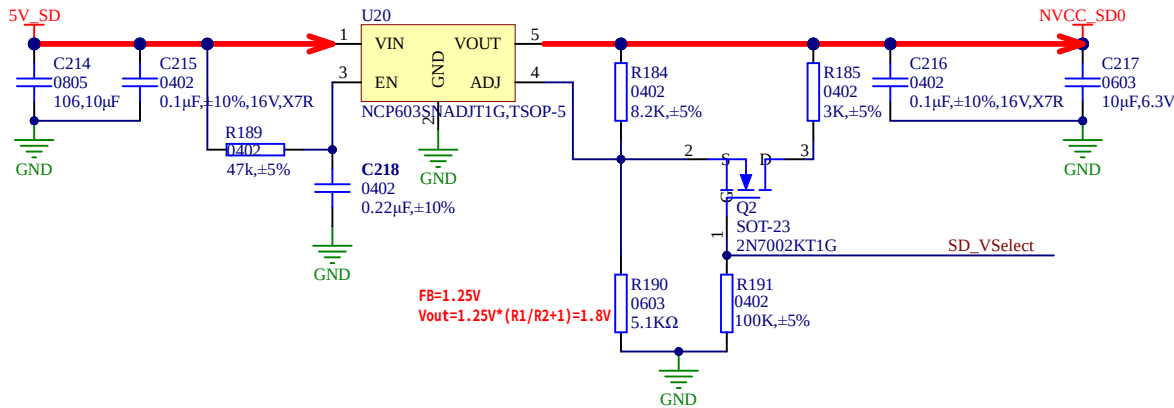
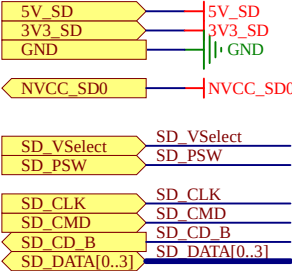


(16-2) USB_HOST2



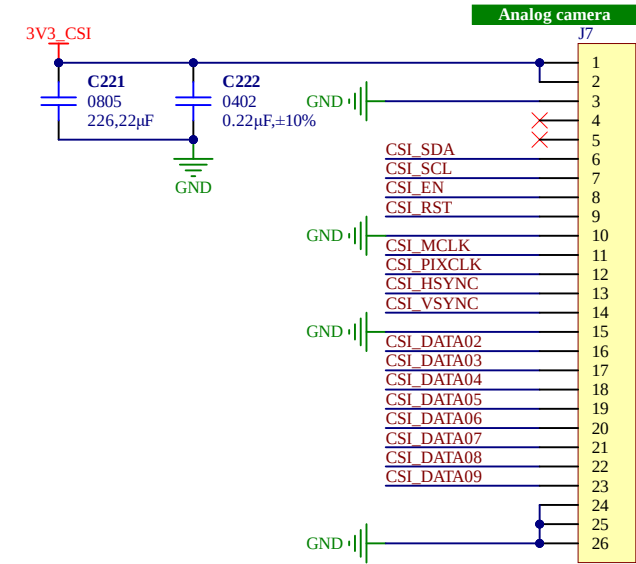
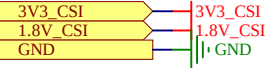
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(17-1) SD

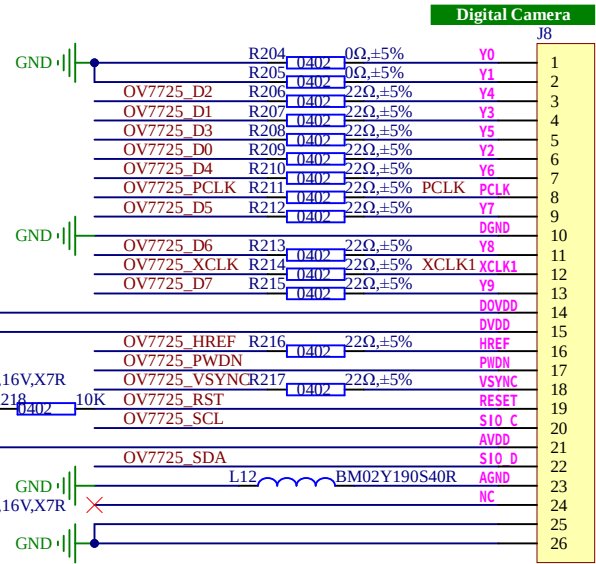
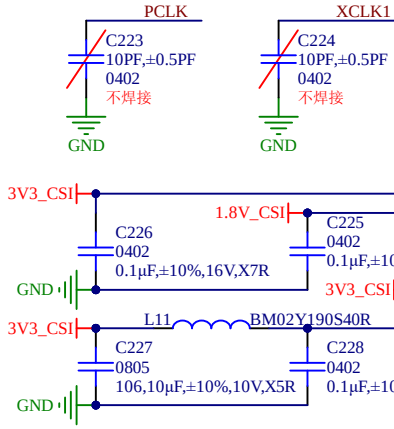


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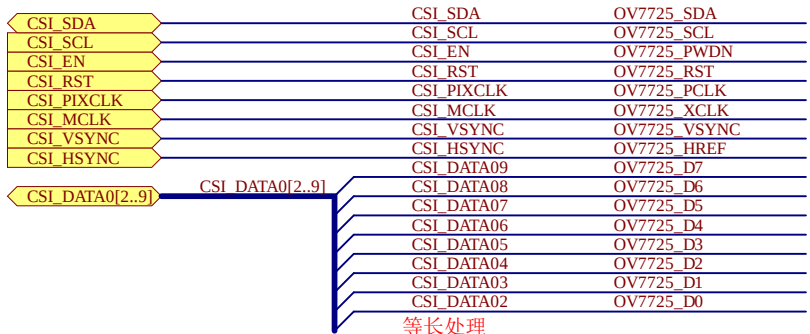
(18-1) CSI



0.5FFC-24PIN
座子, 1.10.01.0133
软排线, 1.11.07.0148
底层放置

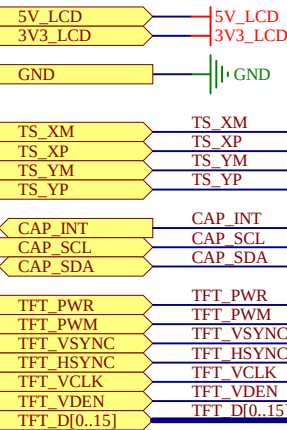


0.5FFC-24PIN
座子, 1.10.01.0133
软排线, 1.11.07.0148
顶层放置

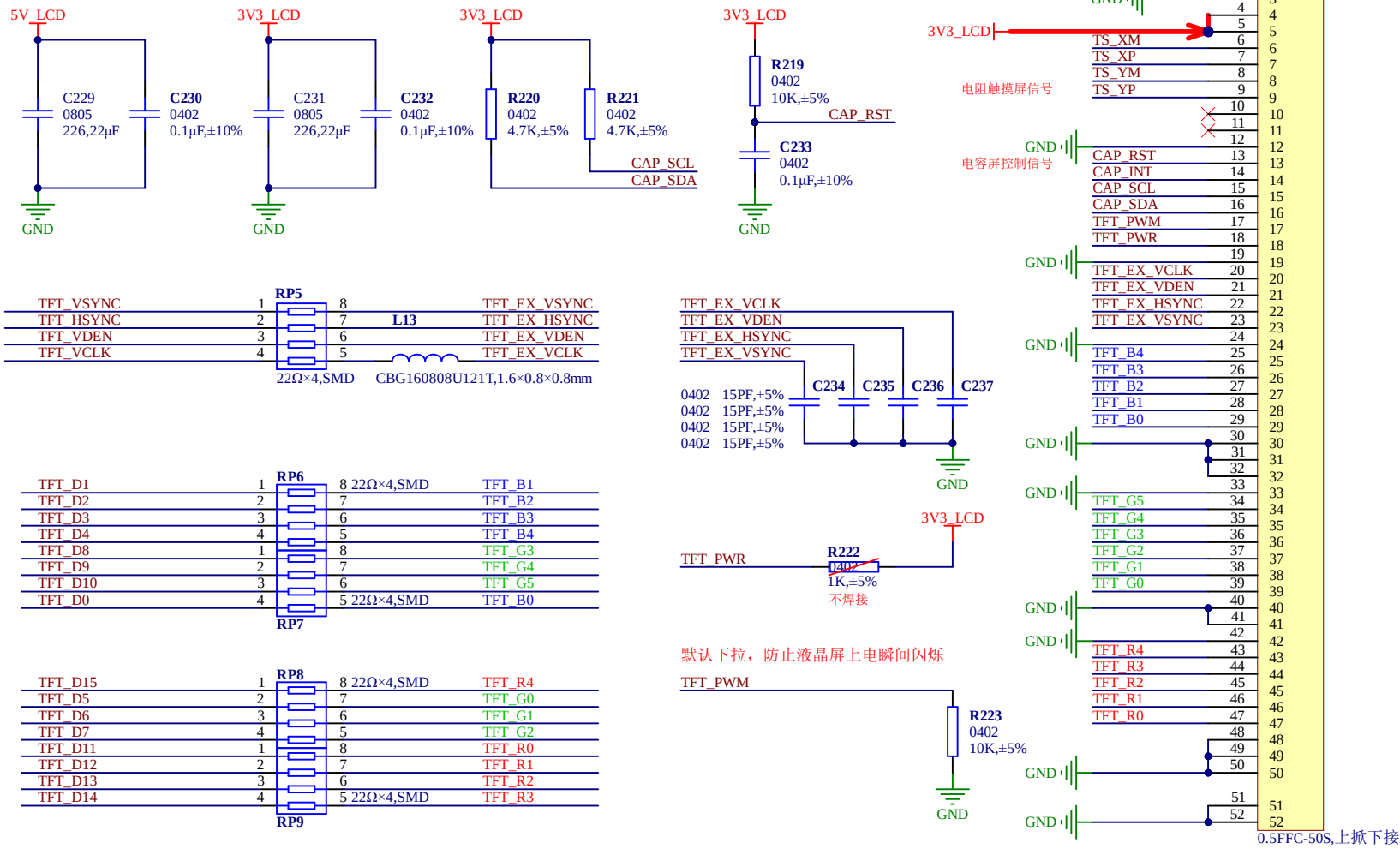


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19.LCD_RGB565

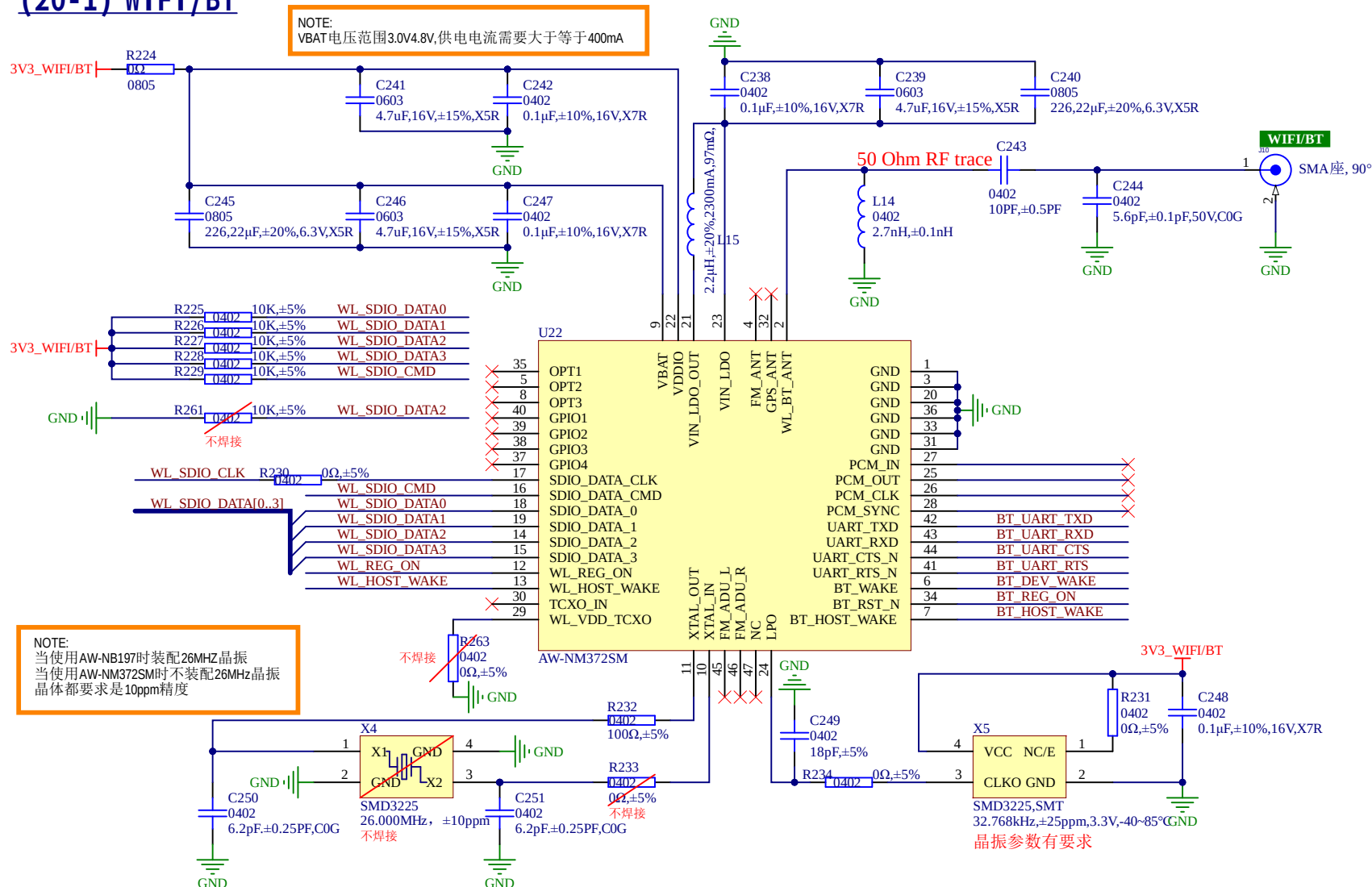
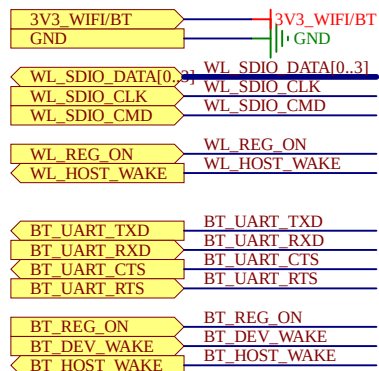


(19-1) LCD RGB565



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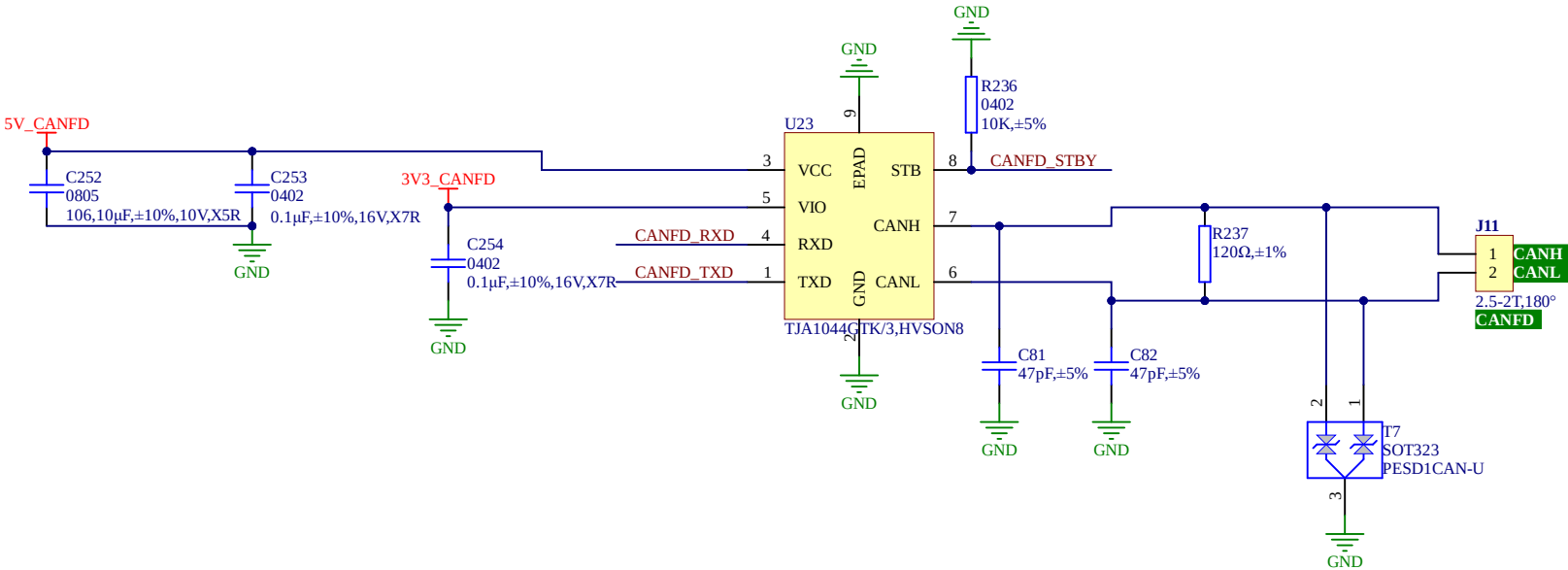
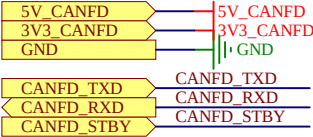
(20-1) WIFI/BT



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21.CANFD_TJA1051T1

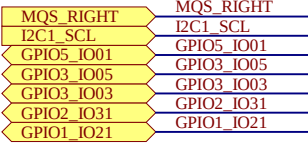
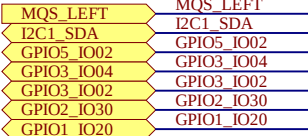
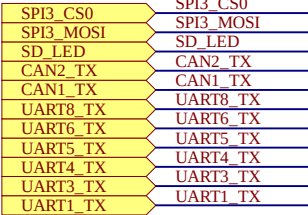
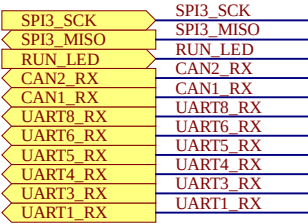
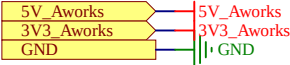
(21-1) CANFD



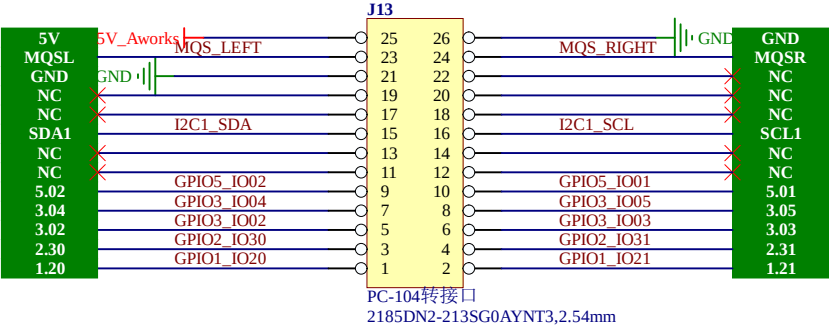
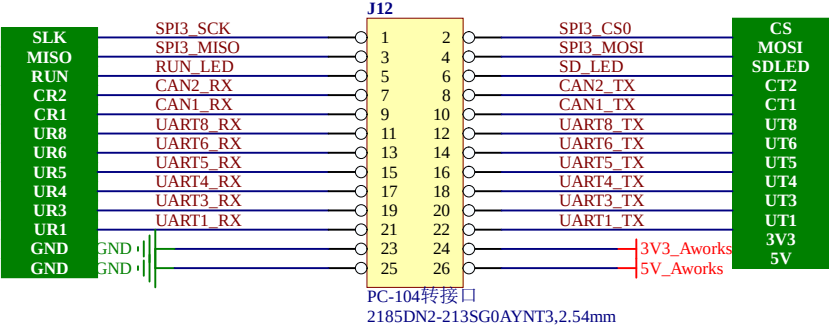
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23.Aworks-Port

(23-1) Aworks-Port

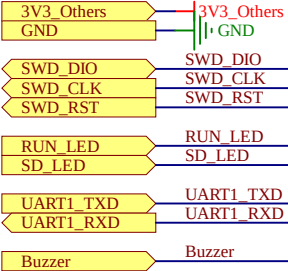


NOTE:
1、注意RT系列主板与配板的引脚的兼容性。
2、IO口功能不局限于此，可通过找到对应IO口复用为其它功能。

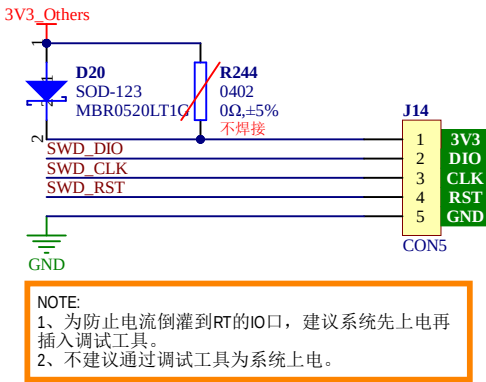


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24.Others



(24-1) SWD

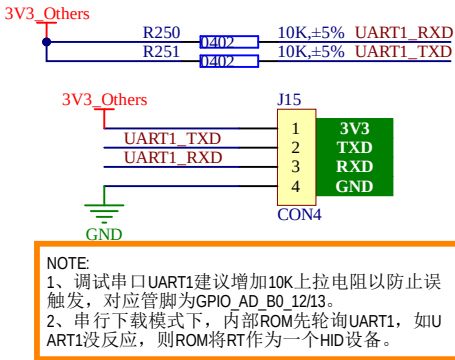


(24-2) LED

NOTE:
1、建议RT的IO口的拉电流与灌电流不要超过1个mA。
2、当拉电流或灌电流较小，且驱动数量较少时可直接驱动。
3、当拉电流或灌电流较大时建议使用驱动电路。

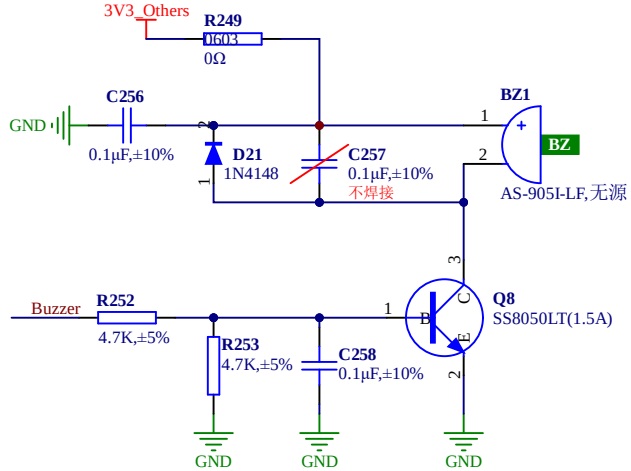


(24-3) UART1



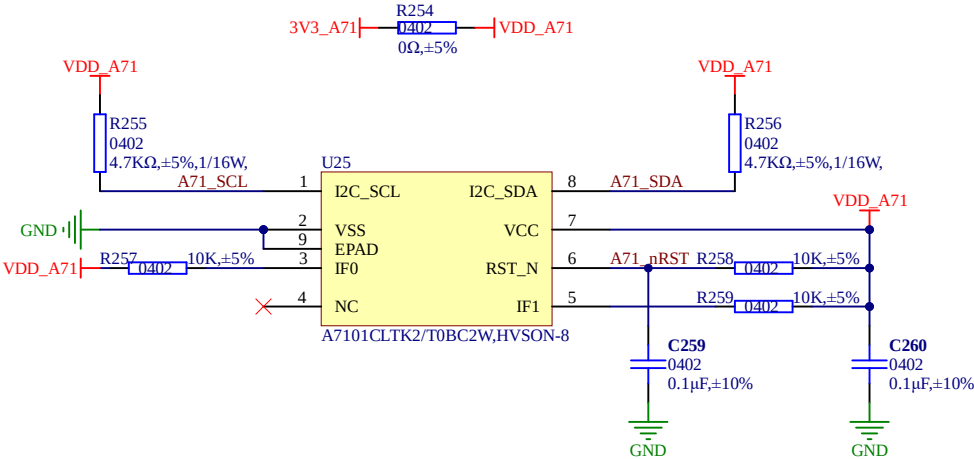
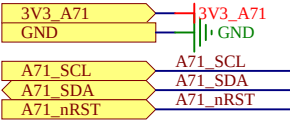
1.UART1	The Serial Downloader provides a means to download a program image to the chip over the USB and UART serial connections. In this mode, ROM programs WDOG1 for a time-out specified by the fuse WDOG Time-out Select (See the Fusemap chapter for details) if the WDOG_ENABLE eFuse is 1 and continuously polls for the USB and UART connection. If no activity is found on USB OTG1 and UART 1/2 and the watchdog timer expires, the Arm core is reset.	The ROM code firstly polls the UART1 signals from TXD1/RXD1. Add a 10-kΩ pull up resistor to the TXD1/RXD1 pins to avoid an invalid trigger of the UART port in the serial download mode.
2. USB1		If there is no polling activity from UART1 in the serial download mode, the ROM code acts as an HID device for PC downloading.

(24-4) Buzzer



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25.EI_A71



#	修改日期	修改内容
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