Rain and Light Sensor with LIN SBC E527.05

PRODUCT PREVIEW – May 28, 2015

RoHS compliant

Features

- Front end rain sensor amplifier
- Four input channels for ambient light measurements
- High sensitivity.
- Very high robustness against sun light
- Configurable µC window watchdog
- LIN Transceiver (V2.1, SAEJ2602, ISO9141)
- Two embedded LED Drivers, driving up to 40mA
- SPI Interface
- Temperature Sensor
- Extensive Diagnosis
- Few external components
- AEC-Q100 Qualification

Applications

- Optical rain sensing to control wiping systems
- Ambient light measurements to control
  - Headlights
  - Head-up Displays
  - Air Conditioning
- Pollution Sensor

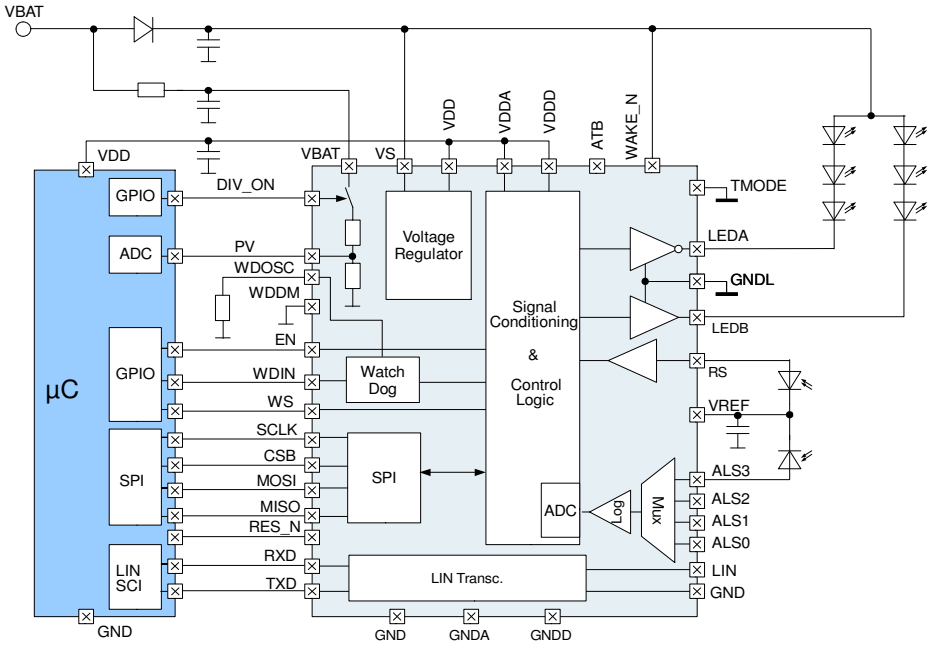
General Description

The RL IC (Rain and Light Sensor) is intended for controlling an optical sensor unit in automotive wiping systems. It provides two embedded LED drivers for stimuli generation. A special, high-sensitive receiver allows processing of a diode input signal without total reflection of the send signal, allowing reliable detection of rain. Due to the used HALIOS®-SD measurement method a very high robustness against sun light is provided. The device has four additional input channels for ambient light measurements.

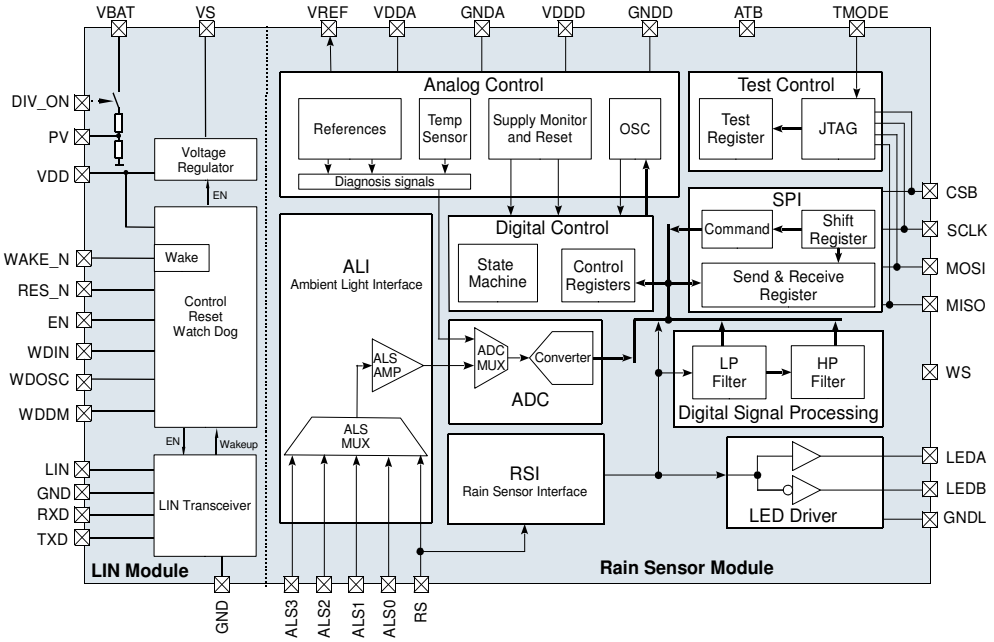
Ordering Information

Ordering-No.:	$Temp_{Junc}$ Range	Package
E52705A39B	-40°C to +105°C	QFN44L7

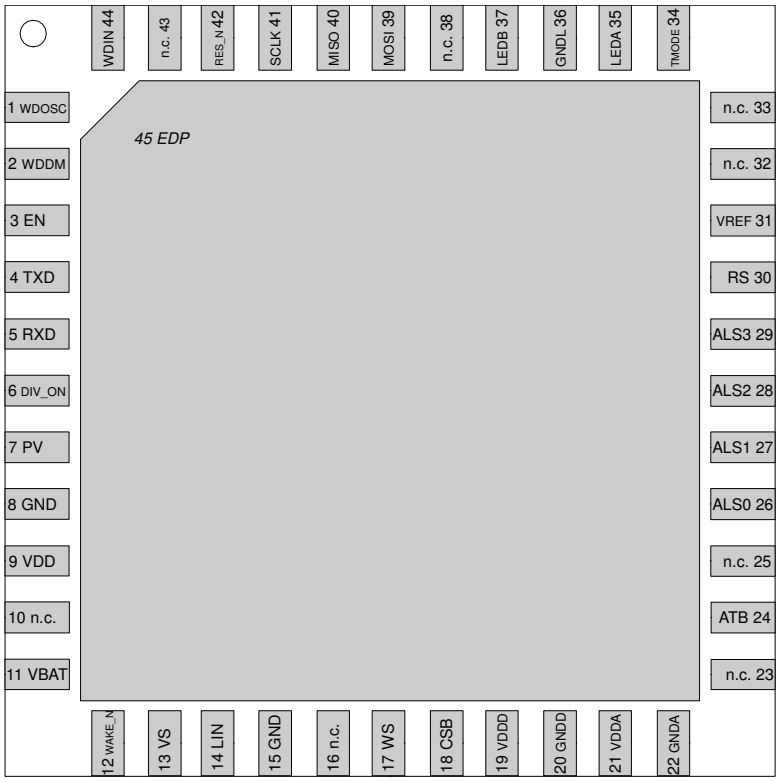
Typical Operating Circuit



Functional Diagram



Pin Configuration QFN44L7



Pin Description QFN44L7

No	Name	Type	Description
1	WDOSC	A_I	watchdog cycle time configuration
2	WDDM	D_I	watchdog debug mode; internal pull down
3	EN	D_I	enable input; internal pull down
4	TXD	D_IO	data transmit; internal pull up; open drain
5	RXD	D_O	receive data output; internal pull up; open drain
6	DIV_ON	D_I	Input to switch on the internal voltage divider; active high; internal pull down
7	PV	A_O	Voltage divider output
8	GND	S	ground
9	VDD	S	3.3V voltage regulator output
10	n.c.		not connected
11	VBAT	HV_S	Battery supply for the voltage divider
12	WAKE_N	HV_D_I	local wake up input; internal pull up to VS
13	VS	HV_S	battery supply voltage
14	LIN	HV_A_IO	LIN bus terminal
15	GND	S	ground
16	n.c.		not connected
17	WS	AD_IO	Digital output pin; internal pull down if not configured as digital output or analog pin (digital and analog test bus during test mode)
18	CSB	D_I	SPI chip select; low active; internal pull up (JTAG pin TMS during test mode)
19	VDDD	S	Digital supply voltage
20	GNDD	S	Digital ground
21	VDDA	S	Analog supply voltage
22	GNDA	S	Analog ground
23	n.c.		not connected
24	ATB	A_IO	not used; internal pull down (analog test bus during test mode)
25	n.c.		not connected
26	ALS0	A_I	Ambient light input current 0; Input for signal current of Ambient Light Sensor 0
27	ALS1	A_I	Ambient light input current 1; Input for signal current of Ambient Light Sensor 1
28	ALS2	A_I	Ambient light input current 2; Input for signal current of Ambient Light Sensor 2
29	ALS3	A_I	Ambient light input current 3; Input for signal current of Ambient Light Sensor 3
30	RS	A_I	Rain sensor input current of receiver diode
31	VREF	A_O	Reference voltage to supply the sensor photo diodes
32	n.c.		not connected
33	n.c.		not connected
34	TMODE	D_I	Test mode enable; active high; internal pull down; when low the JTAG and TMR are hold in reset
35	LEDA	HV_A_O	LED driver output; emitting path A
36	GNDL	S	LEDA/LEDB power ground

No	*Name*	*Type*	*Description*
37	LEDB	HV_A_O	LED driver output; emitting path B
38	n.c.		not connected
39	MOSI	D_I	SPI serial data input; internal pull down; master out - slave in (JTAG pin TDI during test mode)
40	MISO	D_O	SPI serial data output; master in - slave out (JTAG pin TDO during test mode)
41	SCLK	D_I	SPI serial clock; internal pull down (JTAG pin TCK during test mode)
42	RES_N	D_O	reset output; internal pull up; open drain
43	n.c.		not connected
44	WDIN	D_I	watchdog trigger input; internal pull down
45	*EDP*	S	Exposed die pad; has to be connected to large copper PCB ground plane for optimal heat dissipation.

Note: A = Analog, D = Digital, S = Supply, I = Input, O = Output, B = Bidirectional, HV = High Voltage

1 Functional Safety

The development of this product is based on a process according to an ISO/TS 16949 certified quality management system. Functional safety requirements according to ISO 26262 have not been submitted to Elmos and therefore have not been considered for the development of this product.

2 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

No.	Description	Condition	Symbol	Min	Max	Unit
1	Supply voltages VDDA and VDDD		$V_{DDx,MAX}$	-0.3	3.6	V
2	Voltage at pins related to VDDA: ATB		$V_{A,IO,MAX}$	-0.3	VDDA+0.3 but <3.6	V
3	Voltage at pins related to VDDD: SCLK, MISO, MOSI, CSB, WS		$V_{D,IO,MAX}$	-0.3	VDDD+0.3 but <3.6	V
4	Voltage at pin VREF		$V_{REF,MAX}$	-0.3	3.6	V
5	Voltage at pins related to VREF: RS, ALS0 ,ALS1, ALS2, ALS3		$V_{REF,IO,MAX}$	-0.3	VREF+0.3 but <3.6	V
6	Voltage at pin TMODE		$V_{TMODE,MAX}$	-0.3	3.6	V
7	Voltage at pins LEDA and LEDB		$V_{LEDx,MAX}$	-0.3	40	V
8	Current into any ALS pin		$I_{ALSx,MAX}$	-	1.5	mA
9	Current into pin RS		$I_{RS,MAX}$	-	1.5	mA
10	Power dissipation		P_{TOT}	-	tbd.	W
11	Junction temperature		$T_{J,MAX}$	-40	150	℃
12	Storage temperature		T_{STG}	-40	125	℃
13	DC voltage at pin VS, including load dump	continuous	$V_{S,DC}$	-0.3	40	V
14	DC voltage at pin WAKE_N	continuous, 3.3kΩ pre-resistor and 22nF capacitance required, 33kΩ pull-up resistor recommended	$V_{WAKE\_N,DC}$	-2	V_S + 0.3	V
15	DC current at pin WAKE_N	continuous	$I_{WAKE\_N,DC}$	-10	10	mA
16	DC voltage at pin VDD	continuous	$V_{DD,DC3.3}$	-0.3	3.6	V
17	DC current at pin VDD	continuous	$I_{DD,DC}$	-130	1	mA
18	DC input voltage at pin LIN, VBAT	continuous	$V_{LIN,DC}$	-24	40	V
19	TRAN input voltage at pin LIN, VBAT	pulse for max. 500ms	$V_{LIN,TRAN}$	-27	40	V
20	DC Voltage Level for pin EN,RES_N,RXD,TXD,WDIN,WDOSC,WDDM,DIV_ON	continuous	$V_{IO,DC}$	-0.3	$V_{DD,DC}$+0.3	V
21	DC Current Level for pin EN,RES_N,RXD,TXD,WDIN,WDOSC,WDDM,DIV_ON	continuous	$I_{IO,DC}$	-10	1	mA

Stresses beyond these absolute maximum ratings listed below may cause permanent damage to the device. **These are stress ratings only; operation of the device at these or any other conditions beyond those listed in the operational sections of this document is not implied.** Exposure to absolute maximum rated conditions for extended periods may affect device reliability. All voltages referred to VGND. Currents flowing into terminals are positive, those drawn out of a terminal are negative.

3 ESD

Table 3-1: ESD Ratings Table

Description	*Condition*	*Symbol*	*Min*	*Max*	*Unit*
ESD HBM protection at pins LEDA, LEDB	AEC-Q100-002 (HBM), C=100pF, R=1.5kΩ chip level	$V_{ESD(HBM)}$	-2	+2	kV
ESD HBM protection at all other pins	AEC-Q100-002 (HBM), C=100pF, R=1.5kΩ chip level	$V_{ESD(HBM)}$	-2	+2	kV
ESD CDM protection at all pins	AEC-Q100-011 (CDM), R=1Ω chip level	$V_{ESD(CDM)}$	-500	+500	V
ESD protection at pin LIN	AEC-Q100-002 (HBM), C=100pF, R=1.5kΩ chip level	VLIN,ESDHBM to GND	-8	+8	kV
ESD protection at pin LIN 1)	IEC 61000-4-2 C=150 pF, R=330Ω	VLIN,ESD to GND	-8	+8	kV

1) verified with capacitor of CLIN=0pF, CLIN=220pF at pin LIN,CVS,RF=100nF at pin VS and CWAKE_N=22nF, RWAKE_N=3.3kΩ at pin WAKE_N

4 Recommended Operating Conditions

Table 4-1: Recommended Operating Conditions

No.	*Description*	*Condition*	*Symbol*	*Min*	*Typ*	*Max*	*Unit*
1	Supply voltage pin VDDA		V_{DDA}	3.1	3.3	3.5	V
2	Supply Voltage pin VDDD		V_{DDD}	3.1	3.3	3.5	V
3	Difference between supply voltages VDDA and VDDD		$DELTA_{VDDx}$	-0.3	0	0.3	V
4	Current into any ALS pin		I_{ALSx}	1n	-	1m	A
5	Current into pin RS		I_{RS}	1n	-	1m	A
6	Ambient operating temperature		T_{AMB}	-40		+105	℃
7	DC voltage at pin VS		$V_{S,FUNC}$	5	-	28	V
8	DC voltage at pin VS with limited functional range; no system reset occurs	-60mA < I_{DD}	$V_{S,FL,LR}$	3.8	-	7	V
9	DC voltage at pin VS with limited functional range; no system reset occurs	-60mA < I_{DD}	$V_{S,FL,HR}$	18	-	40	V
10	maximum IO current at each pin, if not specified otherwise		$I_{IO,LUP}$	-10	-	10	mA

5 Electrical Characteristics

(V_{VDDx} = 3.1V to 3.5V, T_{amb}=-40°C to + 105°C, unless otherwise noted. Typical values are at V_{VDDx}=3.3V and T_{amb}=+25°C. Positive currents flow into the device pins.)

5.1 Rain Sensor Module

5.1.1 Supply Monitor

Table 5.1.1-1: Electrical Parameters of Supply Monitor

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	VDDA voltage threshold to set MON_C_VDDA comparator output from low to high	VDDA rising edge	$V_{POK,VDDA,RISE}$	2.75	2.9	3.05	V
2	VDDA voltage threshold to set MON_C_VDDA comparator output from high to low	VDDA falling edge	$V_{POK,VDDA,FALL}$	2.7	2.85	3.0	V
3	VDDD voltage threshold to set MON_C_VDDD comparator output from low to high[1)]	VDDD rising edge	$V_{POK,VDDD,RISE}$	2.60	2.8	3.0	V
4	VDDD voltage threshold to set MON_C_VDDD comparator output from high to low[1)]	VDDD falling edge	$V_{POK,VDDD,FALL}$	2.5	2.67	2.85	V
5	VDDA overvoltage threshold	VDDA rising and falling edge	$V_{OV,VDDA}$	3.55	3.85	4.15	V

[1)] measured with VDDA = VDDD ramp

5.1.2 References

Table 5.1.2-1: Electrical Parameters of References

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Internally generated reference voltage at pin VREF		V_{REF}	1.288	1.388	1.488	V
2	Guaranteed current range supplied by pin VREF		I_{VREF}	-3	-	0.2	mA
3	Current into pin VREF in case of VREF shorted to GND		$I_{VREF,SC,GND}$	-25	-16.3	-	mA
4	Current into pin VREF in case of VREF shorted to VDDx		$I_{VREF,SC,VDD}$	-	0.8	2	mA
5	Internally generated reference voltage for ADC		$V_{REF,ADC}$	2.270	2.460	2.610	V

5.1.3 Temperature Sensor

Table 5.1.3-1: Electrical Parameters of Temperature Sensor

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Output voltage of temperature sensor at 25°C		$V_{TEMP,25}$	tbd	(1.24) tbd.	tbd	V
2	Slope of temperature sensor output voltage over absolute temperature[*)]		$SLOPE_{VTEMP}$	tbd	-3.9	tbd	mV/K

[*)] Not tested in production

5.1.4 Oscillator

Table 5.1.4-1: Electrical Parameters of Oscillator

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Trimmed clk frequency		$F_{CLK,TRIM}$	7.2	8	8.8	MHz
2	Number of trimming positions for F_{CLK}*)		$N_{OSC,PROG}$	-	32	-	

*) Not tested in production

5.1.5 Ambient Light Interface (ALI)

Table 5.1.5-1: Electrical Parameters of ALI

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	$\frac{I_{REF,ALI,HI}}{I_{CAL,ALI,HI}}$		$Ratio_{HI}$		4		A/A
2	$\frac{I_{REF,ALI,LO}}{I_{CAL,ALI,LO}}$		$Ratio_{LO}$		0.25		A/A
3	Valid input current for $I_{REF,ALI,LO}$ and $G_{ALI,LO}$1)	Iref=LO, Gain=LO	$I_{PHOTO,ILO,GLO}$	1n		300u	A
4	Time to valid ADC value*)	I_{PHOTO} from 300uA to 1nA. Leakage << 1nA.	$t_{ALI,VALID}$			13.1	ms
5	Time between measurement of two consecutive AUTOMODE ALS measurements.*)		$t_{ALI,AUTOM}$		1		ms
6	Measured current at I_{PHOTO}=1nA, Iref=LO, Gain=LO, known temperature and V_{ref}, without leakage and without further calibration*)	Iref=LO, Gain=LO, I_{PHOTO}=1nA, Temp < 125°	$I_{MEAS,1n}$	0.5		1.5	nA
7	Measured current at I_{PHOTO}=1uA, Iref=LO, Gain=LO, known temperature and V_{ref} and without further calibration	Iref=LO, Gain=LO, I_{PHOTO}=1uA, Temp < 125°	$I_{MEAS,1u}$	0.7		1.5	uA
8	Measured current at I_{PHOTO}=300uA, Iref=LO, Gain=LO, known temperature and V_{ref} and without further calibration	Iref=LO, Gain=LO, I_{PHOTO}=300uA, Temp < 125°	$I_{MEAS,300u}$	270		530	uA

*) Not tested in production
1) production test only with 10nA and 300uA

5.1.6 Rain Sensor Interface (RSI)

Table 5.1.6-1: Electrical Parameters of RSI

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	Minimal adjustable gain of RSI1)		$G_{RSI,LO}$	tbd	100	tbd	dBΩ
2	Maximal adjustable gain of RSI		$G_{RSI,HI}$	tbd	142	tbd	dBΩ
3	Step width of RSI gain setting		$G_{RSI,STEP}$	tbd	2.8	tbd	dBΩ
4	Number of trimming positions for gain of RSI*)		N_{GRSI}	-	16	-	-

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
5	Modulator frequency of RSI*)	FREQ_SHIFT[2:0] = b000	$f_{RSI,MOD}$	90	100	110	kHz
6	Modulator frequency of RSI with max. frequency shift*)	FREQ_SHIFT[2:0] = b111	$f_{RSI,MOD,LO}$	76.60	85.11	93.62	kHz
7	Max. bandwidth of RSI*)		$f_{RSI,BW}$	167	-	-	Hz

*) Not tested in production
1) DC current > 1uA

5.1.7 LED Driver

Table 5.1.7-1: Electrical Parameters of LED Driver

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	output current range of pins LEDA and LEDB		I_{LEDx}			40	mA
2	Current step size of pins LEDA and LEDB		$I_{LEDx,STEP}$		2.5		mA
3	Number of trimming positions of I_{LEDx}*)		$N_{LEDx,STEPS}$	-	16	-	
4	Voltage at pins LEDA and LEDB*)		V_{LEDx}	0.8		18	V
5	Power dissipation at pin LEDA or LEDB*)	$P_{LEDx} = V_{LEDx} * I_{LEDx}$	P_{LEDx}			(0.54) tbd.	W
6	Current slew rate of pins LEDA and LEDB	measured between 20% and 80% of I_{LEDx}	$I_{LEDx,SLEW}$	tbd	tbd	(90) tbd	mA/us
7	Current flowing into pins LEDx while driver is off		$I_{LEDx,LOW}$		(200) tbd.		uA

*) Not tested in production

5.1.8 Serial Peripheral Interface (SPI)

Table 5.1.8-1: Electrical Parameters of SPI

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	CSB, SCLK, MOSI input level low		$V_{IL(SPI)}$			0.3	V_{VDDD}
2	CSB, SCLK, MOSI input level high		$V_{IH(SPI)}$	0.7			V_{VDDD}
3	MISO output level low	$\|I_{OL(SPI)}\| < 2$ mA	$V_{OL(SPI)}$			0.1	V_{VDDD}
4	MISO output level high	$\|I_{OL(SPI)}\| < 2$ mA	$V_{OH(SPI)}$	0.9			V_{VDDD}
5	SPI clock frequency	$C_{LOAD,MISO} \leq 50$pF	$f_{SCLK} = 1 / t_{C(SCLK)}$			1	MHz
6	MOSI setup time*) 1)		$t_{SU(MOSIV)}$	20			ns
7	CSB to MISO time*) 1)		$t_{EN(CSBL-MISOV)}$			225	ns
8	SCLK to MISO time*) 1)		$t_{A(SCLK-MISOV)}$			80	ns
9	Time between two SPI frames*) 1)		$t_{W(CSBH)}$	1			us
10	Maximum allowed time between two SCLK edged.*)		$t_{TO(SPI)}$		1		ms

*) Not tested in production
1) Also holds when the CSB pin is tied to zero.

5.2 LIN Module

5.2.1 Power Supply and References; pin VS

Table 5.2.1-1: DC Characteristics

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	current consumption in active mode	LIN dominant, I_{DD}=0mA	$I_{S,ACT,DOM}$	-	-	5	mA
2	current consumption in active mode	LIN recessive, I_{DD}=0mA	$I_{S,ACT,REC}$	-	-	2	mA
3	standby current	standby mode, V_S =V_{LIN} =V_{WAKE_N} =13.5V, I_{DD}=0mA, T_{AMB}<85°C	$I_{S,STBY}$	-	70	98	µA
4	sleep current	sleep mode, LIN recessive, V_S =V_{LIN} =V_{WAKE_N} =13.5V	$I_{S,SLEEP}$	-	10	20	µA
5	sleep current, LIN is neither recessive nor dominant, not production tested*)	sleep mode, LIN is floating V_S =V_{WAKE_N} =13.5V, T_{AMP} > 40°C	$I_{S,SLEEP,LIN}$	-	-	60	µA
6	sleep current	sleep mode, LIN is floating V_S =V_{WAKE_N} =13.5V, V_{LIN} > $V_{LIN,THDOM}$	$I_{S,SLEEP,40C}$			25	µA

*) Not tested in production

5.2.2 LIN Module Operating Modes

Table 5.2.2-1: AC Characteristics

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	debounce filter for active mode transition		t_{2AM}	23	25	44	µs
2	debounce filter for standby mode transition		t_{2STBY}	23	25	44	µs
3	debounce filter for sleep mode transition		t_{2SLEEP}	23	25	44	µs
4	debounce filter for flash mode transition		t_{2FM}	2	4	6	µs
5	open window for flash mode acknowledge		t_{FMACK}	3	-	-	µs
6	flash mode time out		t_{FMTO}	1.2		2	ms
7	delay for switching off the VDD regulator after entering sleep mode		$t_{DD,OFFDEL}$	64	128	-	µs

5.2.3 Fail Safe System

5.2.3.1 Reset Parameters

Table 5.2.3.1-1: DC Characteristics Reset

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	power on reset according to pin **VS**		$V_{S,POR}$	4.0	-	5.0	V

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
2	power down threshold according to pin **VS**		$V_{S,PD}$	3.0	-	3.8	V
3	reset assert level at pin **VDD** (3.3V device)		$V_{DD,RSTA3.3}$	2.4	-	2.8	V
4	reset release level at pin **VDD** (3.3V device)		$V_{DD,RSTD3.3}$	2.6	-	3.0	V
5	reset hysteresis at pin **VDD** (3.3V device)*)	$V_{DD,RSTD3.3}$ - $V_{DD,RSTA3.3}$	$V_{DD,HYST3.3}$	100	-	400	mV

*) Not tested in production

Table 5.2.3.1-2: AC Characteristic Reset

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	pin **RES_N** activation time		t_{RES_N}	2	3	5	ms
2	undervoltage debounce time		$t_{RES\_N,RSTA}$	60		90	us

5.2.3.2 Monitor Parameters

Table 5.2.3.2-1: DC Characteristics Monitoring

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	thermal shutdown flag threshold		T_{SHDN}	150	-	180	℃
2	thermal shutdown flag hysteresis.*)		T_{HYST}	5	-	22	K
3	LIN overvoltage condition in dominant state	active mode, **TXD**=0	$V_{LIN,OV}$	-	4	-	V

*) Not tested in production

Table 5.2.3.2-2: AC Characteristics Monitoring

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	LIN over voltage debounce time	LIN dominant	$t_{LIN,OV}$	-	25	-	µs
2	voltage regulator shut down debounce time		$t_{DD,SHDN}$	-	50	-	µs

5.2.4 Wake Up

5.2.4.1 Local Wake Up; pin WAKE_N

Table 5.2.4.1-1: DC Characteristics

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	leakage current	V_{WAKE_N}=V_S=18V	$I_{WAKE\_N,LEAK}$	-5	-	5	µA
2	input low level		$V_{WAKE\_N,INL}$	2.5	3.0	3.5	V
3	input high level		$V_{WAKE\_N,INH}$	3.0	3.5	4.0	V
4	input hysteresis*)		$V_{WAKE\_N,HYST}$	0.2	0.5	0.8	V
5	pull up current	V_S < 28 V, V_{WAKE_N} = 0 V	$I_{WAKE\_N,PU}$	-30	-10	-	µA

*) Not tested in production

Table 5.2.4.1-2: AC Characteristics

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	input debouncing filter time		$t_{WAKE\_N,DB}$	-	-	25	µs

5.2.5 Voltage Regulator; pin VDD

Table 5.2.5-1: DC Characteristics Active Mode

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	output voltage range	active mode	$V_{DD,ACT3.3}$	3.23	3.3	3.37	V
2	output current range with 2% VDD accuracy		$I_{DD,ACT60}$	-60	-	-	mA
3	output current range with 5% VDD accuracy		$I_{DD,ACT100}$	-100	-	-	mA
4	output current limitation		$I_{DD,LIM}$	-230	-	-130	mA
5	Power supply ripple rejection*)	10 Hz to 100 Hz C_{VDD} = 10 µF V_S = 14V, IVDD = 15 mA	PSRR	50			dB

*) Not tested in production

Table 5.2.5-2: DC Characteristics Standby Mode

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	output voltage range*)	standby mode	$V_{DD,STBY3.3}$	3.135	3.3	3.465	V

*) Not tested in production

5.2.6 Watchdog

Table 5.2.6-1: AC Characteristics

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	watchdog period for 10kΩ resistance	R_{WDOSC}=10kΩ	$t_{WD,OSC10k}$	7.2	10	13.2	ms
2	watchdog period for 100kΩ resistance	R_{WDOSC}=100kΩ	$t_{WD,OSC100k}$	88.2	100	112.2	ms
3	first trigger open window	open window after **RES_N** is released	$t_{WD,FIRST}$	91	110	135	ms
4	open window duty		$d_{WD,OW}$	-	50	-	%
5	closed window duty		$d_{WD,CW}$	-	50	-	%
6	watchdog reset time		$t_{WD,RES}$	414	512	645	µs
7	trigger command pulse width		$t_{WD,CMD}$	8	-	-	µs

5.2.7 LIN Transceiver; pin LIN

Table 5.2.7-1: DC characteristics

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	functional range LIN transceiver		$V_{LIN,VS}$	7	-	18	V
2	recessive output voltage	**TXD**=1	$V_{LIN,REC}$	V_S -1V	-	V_S	-
3	dominant output voltage	**TXD**=0, V_S=7.0V, R_{LIN}=0.5kΩ to V_S	$V_{LIN,DOM}$	-	-	1.2	V
4	dominant output voltage	**TXD**=0, V_S=18V, R_{LIN}=0.5kΩ to V_S	$V_{LIN,DOM1}$	-	-	2.0	V
5	receiver dominant level		$V_{LIN,THDOM}$	-	-	0.4	V_S
6	receiver recessive level		$V_{LIN,THREC}$	0.6	-	-	V_S

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
7	LIN bus center voltage	$V_{LIN,BUSCNT}$= ($V_{LIN,THDOM}$+$V_{LIN,THREC}$)/2	$V_{LIN,BUSCNT}$	0.475	-	0.525	V_S
8	receiver hysteresis	$V_{LIN,THREC}$- $V_{LIN,THDOM}$	$V_{LIN,HYS}$	-	-	0.175	V_S
9	output current limitation	V_{LIN} = $V_{VS,MAX}$ = 18 V	$I_{LIN,LIM}$	40	-	200	mA
10	pull up resistance		$R_{LIN,SLAVE}$	20	33	60	kΩ
11	leakage current flowing into pin **LIN**	transmitter passive, 7V<V_S<18V, 7V<V_{LIN}<18V, V_{LIN}>V_S	$I_{LIN,BUSREC}$	-	8	20	µA
12	pull up current flowing out of pin **LIN**	transmitter passive, 7V<V_S<18V, V_{LIN}=0V	$I_{LIN,BUSDOM}$	-1	-	-	mA
13	leakage current, ground disconnected (**GND** device = **VS**)	V_S=13.5V, 0V<V_{LIN}<18V	$I_{LIN,NOGND}$	-1	-	0.1	mA
14	leakage current, supply disconnected	V_S=0V, 0V<V_{LIN}<18V	I_{LIN}	-	8	20	µA
15	leakage current, supply disconnected, T = 85 °C *)	V_S=0V, 0V<V_{LIN}<18V	$I_{LIN,85}$	-	-	15	µA
16	clamping voltage*)	V_S=0V, I_{LIN}=1mA	$V_{LIN,CLAMP}$	40		-	V

*) Not tested in production

Table 5.2.7-2: AC characteristics

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	input capacitance*)	7V < V_S < 18V	$C_{LIN,PIN}$	-	-	30	pF
2	output slew rate	C_{LIN}=1-10nF, R_{LIN}=0.5-1kΩ, 1µs<t_{LIN}<5µs, V_S=18V	$SR_{LIN,OUT}$	1	-	3	V/µs
3	output slew rate	C_{LIN}=1-10nF, R_{LIN}=0.5-1kΩ, 1µs<t_{LIN}<5µs, V_S=7.0V	$SR_{LIN,OUT1}$	0.5	-	3	V/µs
4	symmetry of rising and falling edge	V_S=18V	$t_{LIN,SYM}$	-5	-	5	µs
5	transmit propagation delay, is deleted		$t_{TXD,PDT}$	-	-	4	µs
6	transmit propagation delay symmetry, is deleted		$t_{TXD,SYM}$	-2	-	2	µs
7	receive propagation delay		$t_{RXD,PDR}$	-	-	6	µs
8	receive propagation delay symmetry		$t_{RXD,SYM}$	-2	-	2	µs
9	LIN bus pulse receiver debounce time		$t_{LIN,DB}$	0.3	-	6	µs
10	wake-up debounce time		$t_{LIN,WU}$	70	-	150	µs

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
11	Duty cycle 1 [1)]	$V_{LIN,THREC}$(max) =0.744*V_S, $V_{LIN,THDOM}$(max) =0.581*V_S, V_S=7-18V, t_{BIT}=50µs, $D_{LIN,1}$=t_{BUSREC}(min)/ (2*t_{BIT})	$D_{LIN,1}$	0.396	-	-	-
12	Duty cycle 2 [1)]	$V_{LIN,THREC}$(min) =0.422*V_S, $V_{LIN,THDOM}$(min) =0.284*V_S, V_S=7-18V, t_{BIT}=50µs, $D_{LIN,2}$=t_{BUSREC}(max)/ (2*t_{BIT})	$D_{LIN,2}$	-	-	0.581	-
13	Duty cycle 3 [1)]	$V_{,LIN,THREC}$(max) =0.778*V_S, $V_{LIN,THDOM}$(max) =0.616*V_S, V_S=7-18V, t_{BIT}=96µs, $D_{LIN,3}$=t_{BUSREC}(min)/ (2*t_{BIT})	$D_{LIN,3}$	0.417	-	-	-
14	Duty cycle 4 [1)]	$V_{LIN,THREC}$(min) =0.389*V_S, $V_{LIN,THDOM}$(min) =0.251*V_S, V_S=7-18V, t_{BIT}=96µs, $D_{LIN,4}$=t_{BUSREC}(max)/ (2*t_{BIT})	$D_{LIN,4}$	-	-	0.590	-
15	receive data baud rate	flash mode, V_S=13V	$B_{LIN,RXD}$			250	kBds
16	transmit data baud rate	flash mode, V_S=13V	$B_{LIN,TXD}$			115	kBds

*) Not tested in production

1) Bus load conditions (C_{LIN},R_{LIN}): 1nF, 1kΩ/6.8nF, 660Ω/10nF, 500Ω

5.2.8 IO Peripherals

5.2.8.1 Enable; pin EN

Table 5.2.8.1-1: DC Characteristics

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	input low level range		$V_{EN,INL}$	0	-	0.25	V_{DD}
2	input high level range		$V_{EN,INH}$	0.75		1.0	V_{DD}
3	pull down resistor	V_{EN}=5.0V	$R_{EN,PD}$	80		220	kΩ
4	input leakage	V_{EN}=0V	$I_{EN,LEAK}$	-5	-	5	µA

5.2.8.2 Transmit Data Input; pin TXD

Table 5.2.8.2-1: DC Characteristics

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	input low voltage range		$V_{TXD,INL}$	0	-	0.25	V_{DD}
2	input high voltage range		$V_{TXD,INH}$	0.75	-	1.0	V_{DD}
3	output low level range	I_{TXD}=1mA	$V_{TXD,OUT}$	-0.3	-	0.6	V
4	TXD pull up resistor	V_{TXD}=0V	$R_{TXD,PU}$	80		220	kΩ

Table 5.2.8.2-2: AC Characteristics

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	time out detection of TXD	TXD = 0 V, active mode	$t_{TXD,TO}$	6	10	14	ms

5.2.8.3 Receive Data Output; pin RXD

Table 5.2.8.3-1: DC Characteristics

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	output low level range	I_{RXD}=1mA	$V_{RXD,OUT}$	-0.3	-	0.6	V
2	pull up resistance	V_{RXD}=0V	$V_{RXD,PU}$	3	5	10	kΩ

5.2.8.4 Reset; pin RES_N

Table 5.2.8.4-1: DC Characteristics

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	output low level range	I_{RES_N}=1mA	$V_{RES\_N,OUT}$	-0.3	-	0.6	V
2	pull up resistance	V_{RES_N}=0V	$I_{RES\_N,PU}$	3	5	10	kΩ

5.2.8.5 Watchdog Trigger Input; pin WDIN

Table 5.2.8.5-1: DC Characteristics

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	input low level range		V_{WDIN_INL}	0	-	0.25	V_{DD}
2	input high level range		$V_{WDIN,INH}$	0.75	-	1.0	V_{DD}

5.2.8.6 Watchdog Cycle Time Configuration; pin WDOSC

Table 5.2.8.6-1: DC Characteristics

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	reference current	V_{WDOSC} = 1 V	$I_{WDOSC,REF}$	-	14	-	µA

5.2.8.7 Watchdog Debug Mode; pin WDDM

Table 5.2.8.7-1: DC Characteristics

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	input low level range		$V_{WDDM,INL}$	0	-	0.25	V_{DD}
2	input high level range		$V_{WDDM,INH}$	0.75	-	1.0	V_{DD}

5.2.9 VBAT Voltage divider

Table 5.2.9-1: DC Characteristics

No.	Description	Condition	Symbol	Min	Typ	Max	Unit
1	divider ratio	$V_{s,PD} < V_S < 18$ V	$DR_{PV,3.3V}$	5.86		6.04	
2	V_{BAT} range of divider linearity	$V_{DD} = 3.3$ V	$L_{VBAT,3.3V}$	3.3		18	V
3	divider ratio error*)		DRE_{PV}	-1.5		1.5	%
4	V_{BAT} input current	$V_{BAT} = 13.8$ V	I_{VBAT}		150		µA
5	reverse current	$V_{BAT} = -24$ V	I_{VBAT_REV}	-1			mA
6	Maximum output Voltage at PV	18 V < V_{BAT} < 40 V	$V_{PV,MAX,3.3V}$		1		V_{DD}
7	divider temperature drift*)		T_R		tbd		ppm/K
8	input low level range		$V_{DIV\_ON,INL}$	0		0.25	V_{DD}
9	input high level range		$V_{DIV\_ON,INH}$	0.75		1.0	V_{DD}

*) Not tested in production

6 Functional Description

6.1 Rain Sensor Module

6.1.1 Overview

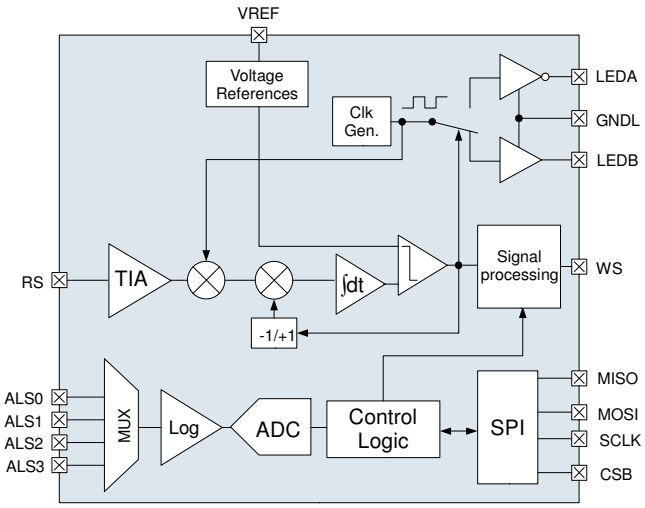


Figure 6.1.1-1: Simplified functional diagram

The purpose of the Rain Sensor Module is to control an optical sensor unit for rain detection and ambient light measurement. The signal flow is displayed in a simplified functional diagram (figure Figure 6.1.1-1).

6.1.1.1 Rain Sensor Interface

The basic principle is a balancing of the light of two led channels (LEDA, LEDB) which are received by one photo diode. Both sending channels send out light pulses triggered by a fixed clock and they are driven by the same current.
The photo current will be integrated and compared with a reference signal. Both channels are not sending simultaneously. It depends on the value of the integrated voltage. If it is greater than the reference voltage channel LEDA will send, if it it is lower than channel LEDB which cause a down integration. That will continue until it comes to a steady state in which the integrated voltage value is toggling around the reference value.

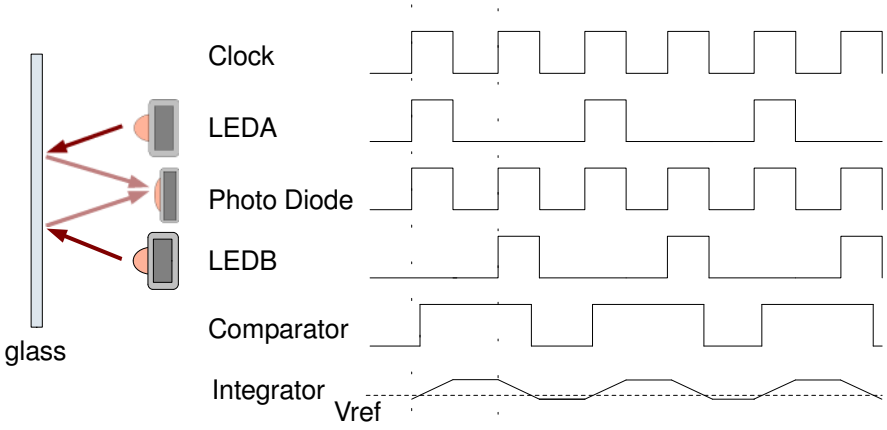


Figure 6.1.1.1-1: Principal signals without water drops

Rain drops will disturb the balance due to the reflection change of the surface. The reflected light of one channel will decrease and new equilibrium has to be found.

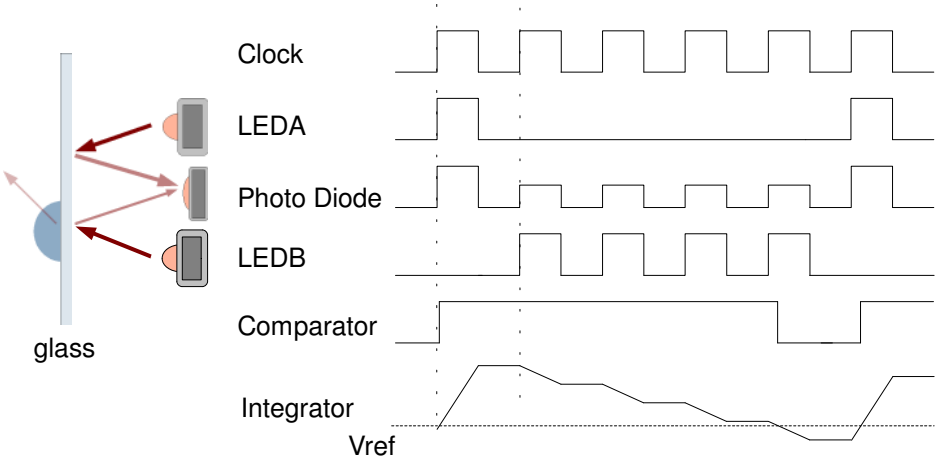


Figure 6.1.1.1-2: Principal signals with water drops

The input amplifier amplifies the photo current and eliminates the DC current part of the photo current, thus the ambient light.
The demodulator blanks out one half of the mirrored input signal. The sign block determines the sign of the current input signal which has to be added in the integrator module. The comparator compares the integrated input signal with the reference voltage and delivers at his output the bit stream. The bit stream is averaged with a low pass filter.

The averaged bit stream value is a non linear function of LEDA and LEDB damping (see figure Figure 6.1.1.1-3). If the photo diode receive the light from both LEDs with the same strength the averaged bit stream value is 0.5. If the light from LEDA (-100% to 0%) is damped by water drop and the light from LEDB not, the averaged bit stream value goes below 0.5. If the light from LEDB (0% to 100%) is damped by water drop and the light from LEDB not, the averaged bit stream value goes above 0.5.

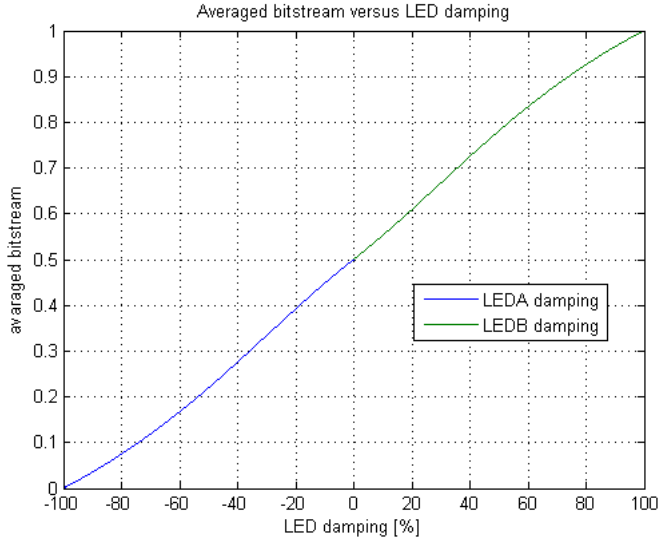


Figure 6.1.1.1-3: Averaged bitstream value as function of LEDA and LEDB damping. Negative x values (blue line) are only LEDA damping, positive x values are only LEDB damping.

6.1.1.2 Ambient Light Interface

For ambient light measurement the Ambient Light Interface (ALI) provides 4+1 channels to read out the current from photo diodes. With a multiplexer the channel is selected. The selected photo current is amplified by a logarithmic amplifier with selectable gain and converted to a voltage. This voltage is sampled with an ADC and the digitized value is optional averaged over several samples.

6.1.2 Supply Monitor

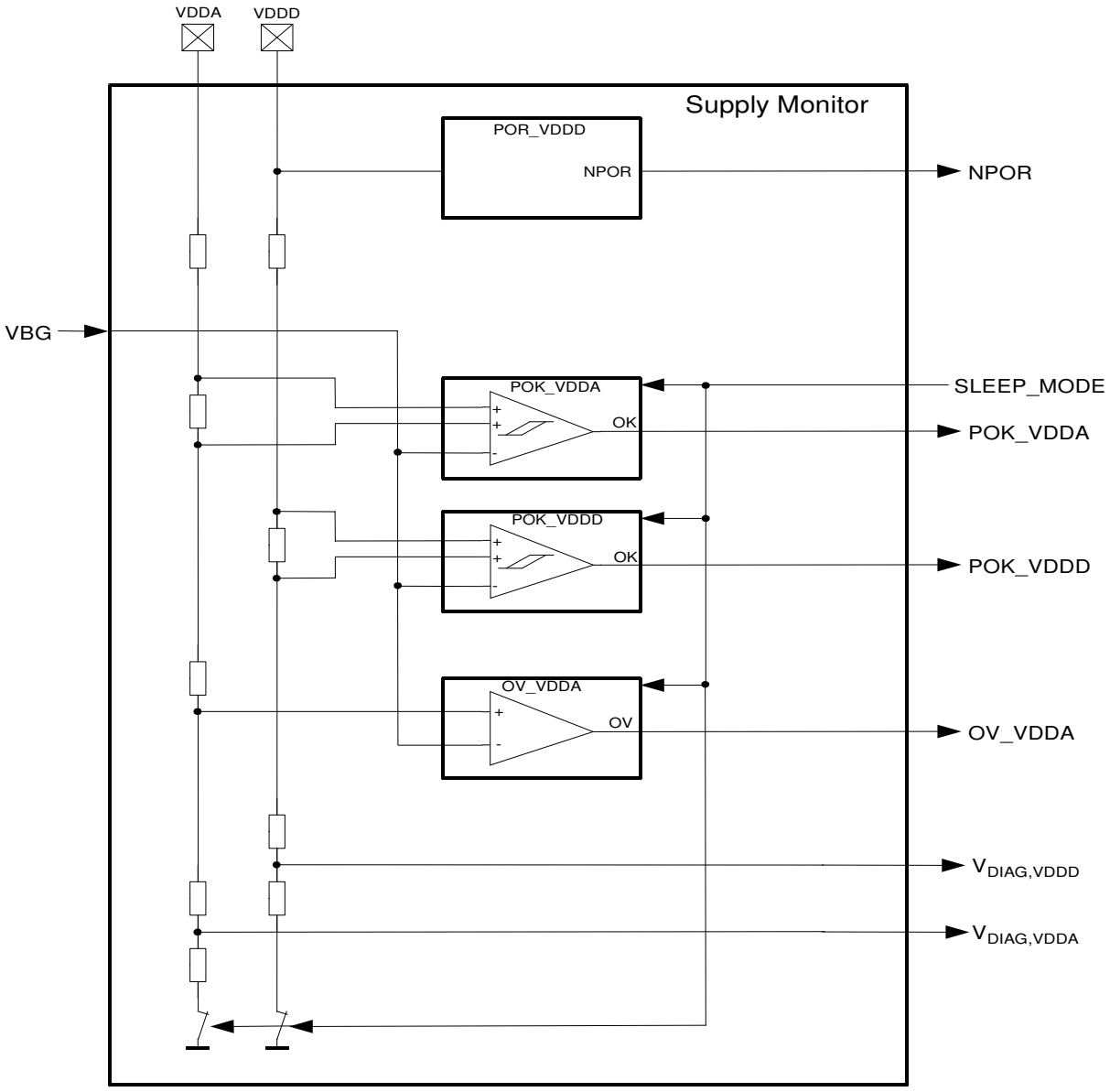


Figure 6.1.2-1: Block Diagram of Supply Monitor and Reset Generation

The supply monitor supervises the external supply voltages VDDA and VDDD:

- In case any supply voltage is lower than expected, reset will be generated
- If VDDA is higher than expected over voltage will be detected

Reset generation
Both supply voltages are compared with a reference voltage.
Comparators POR_VDDD use a reference voltage related to the threshold voltage of the implemented MOS transistors. Thus this reference varies over temperature and process parameters.
Comparators POK_VDDx use a constant reference voltage derived from the bandgap reference.
In order to avoid toggling of the reset signal all comparators contain a hysteresis. For a comparator output signal 'OK=low' ,what is generally the case during power up, the corresponding 'low to high' reference $V_{MON,TH,LH}$, $V_{MON,CA,LH}$ or $V_{MON,CD,LH}$ is selected. During 'OK=high' what is likely the case during power down, the corresponding 'high to low' reference is used.
During start-up it is possible, that POK_VDDD is released early, when VDDA < VDDD so that the bandgap voltage is not ready yet. Since POK_VDDA and POK_VDDD are combined reset sources and POK_VDDA is not released in this condition, this poses no problem. It has to be taken into account during production testing though.
In sleep mode the clock of the digital part is switched off. Thus the requirements concerning the supply voltage decrease as there are no timing constrains. Supply voltage has to be sufficiently high to ensure that all registers keep their value. This can be guaranteed with the comparators MON_VTH_VDDx. So in sleep mode the output signals of comparators MON_C_VDDx are not taken into account for reset generation. Thus these comparators can be switched off in sleep mode in order to reduce current consumption.

Over voltage detection
As both supply voltages are generated externally by a single voltage regulator, it is sufficient to check only one supply against over voltage. As shown in figure Figure 6.1.2-1 VDDA is compared to $V_{MON,OV}$.
In order to reduce current consumption in sleep mode, the comparator MON_OV_VDDA is switched of and it's output 'OV' is disabled. Over voltage will not be detected in sleep mode.

Diagnosis
For diagnosis purpose, the supply voltages can be measured by $V_{DIAG,VDDA}$ and $V_{DIAG,VDDD}$ via internal ADC. These diagnosis voltages are not available in sleep mode.

6.1.2.1 Power-up and -down Timing Diagram

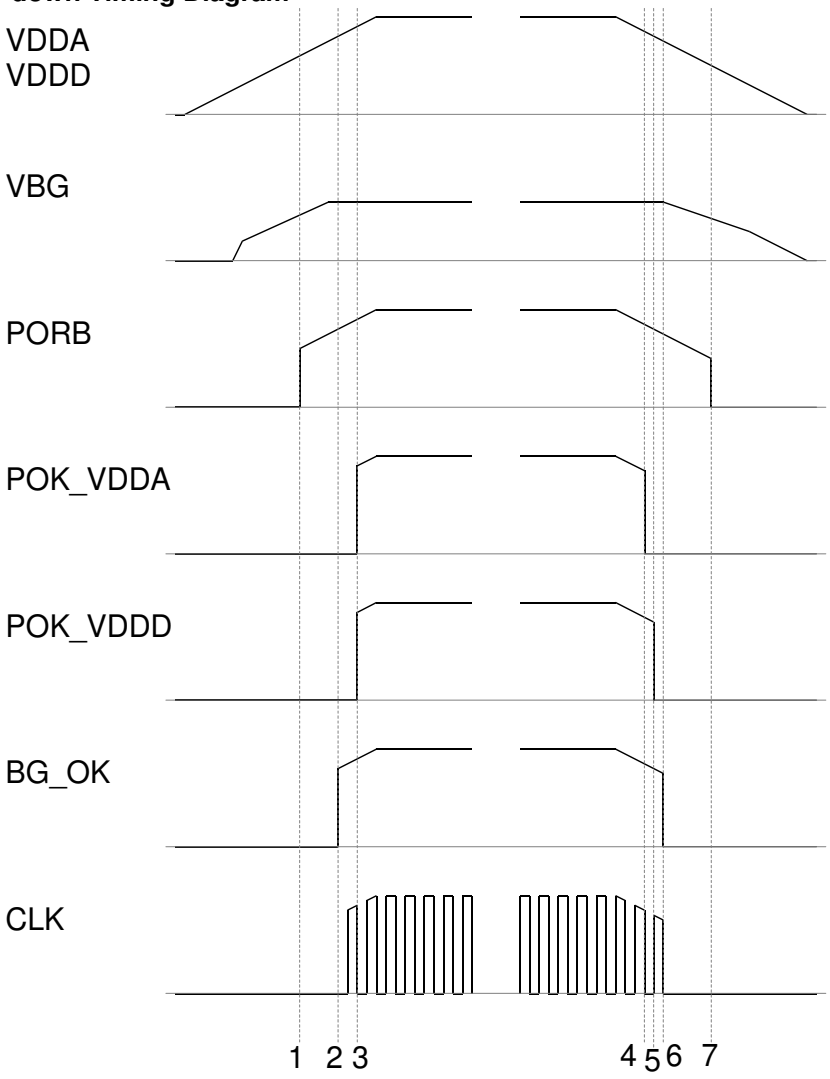


Figure 6.1.2.1-1: Power Timing Diagram

During power-ramp up, several cells ensure a clean start-up of the circuitry. First the POR_VDD comparator holds the whole system in reset until a VDDD crosses the combined threshold voltage of the used MOSFETs (1). At this point, the bandgap-reference is working well enough to generate a stable BG_OK signal. When VBG is stable, BG_OK rises (2) which is ANDed with the supply monitor comparators POK_VDDx, since their thresholds are referenced from VBG. BG_OK also enables the oscillator. Only when POK_VDDD and POK_VDDA are also high, the system is released from its reset-state (3).

When the power falls below the power comparator threshold $V_{MON,CA,HL}$ (4) or $V_{MON,CD,HL}$ (5) respectively, the system is reset until power rises again. If power falls further the bandgap reference cell signals insufficient power by setting BG_OK to 0 (6), which also stops the oscillator. Finally (7) the PORB signal ensures the reset when all other analog ciruitry cannot work due to low power supply voltage.

During sleep mode the bandgap reference and the oscillator are switched of. Since their reference is missing, the POK_VDDx comparators are also powered-down. The only power watch remaining is the POR_VDDD comparator to ensure information stored in registers is kept. If the ASIC exits te sleep mode due to SPI activity and VDDD or VDDA are below their tresholds, the device is reset as soon BG_OK signal rises.

6.1.3 References

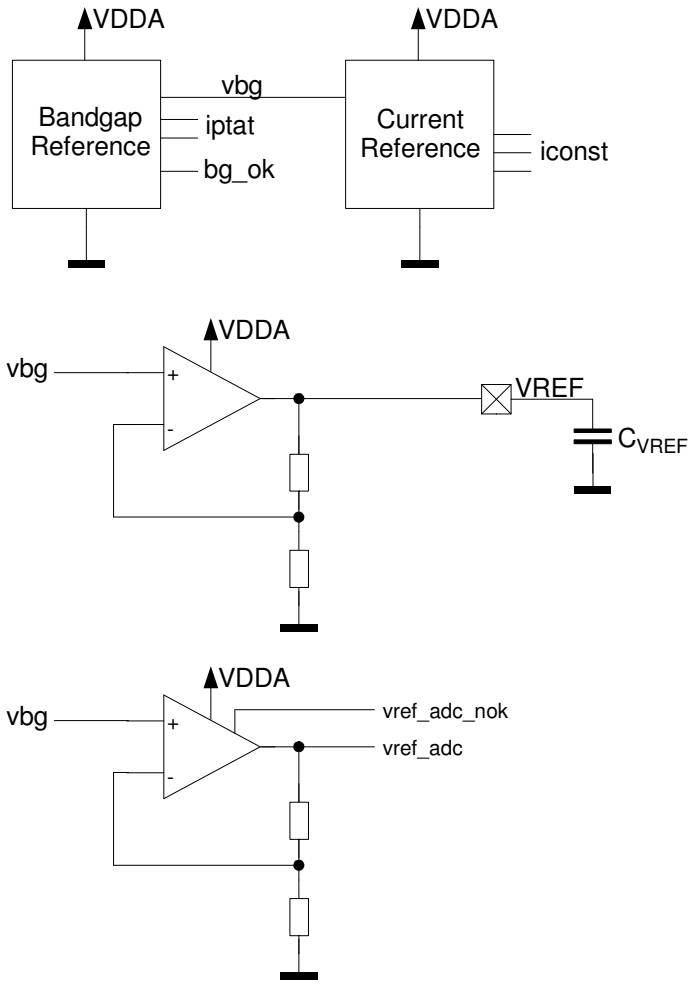


Figure 6.1.3-1: Block Diagram of References

Function of this block is the generation of reference voltages and currents:

- V_{REF}
- $V_{REF,ADC}$

V_{REF}

The internally generated voltage V_{REF} is output at pin VREF. V_{REF} is intended as reference for external photo diodes and the corresponding interface; Rain Sensor Interface and the Ambient Light Interface.
The guaranteed output current range of pin VREF is defined by parameter I_{VREF}.
In case of an external short circuit of pin VREF to VDDx or GNDx the current is limited to $I_{VREF,SC,VDD}$ and $I_{VREF,SC,GND}$ respectively.
The external decoupling capacitor C_{VREF} should be placed as close as possible to the IC pins VREF and AGND.
For diagnosis purpose VREF can be measured by the internal ADC.

$V_{REF,ADC}$

$V_{REF,ADC}$ is the upper reference voltage for the internal ADC.

6.1.4 Temperature Sensor

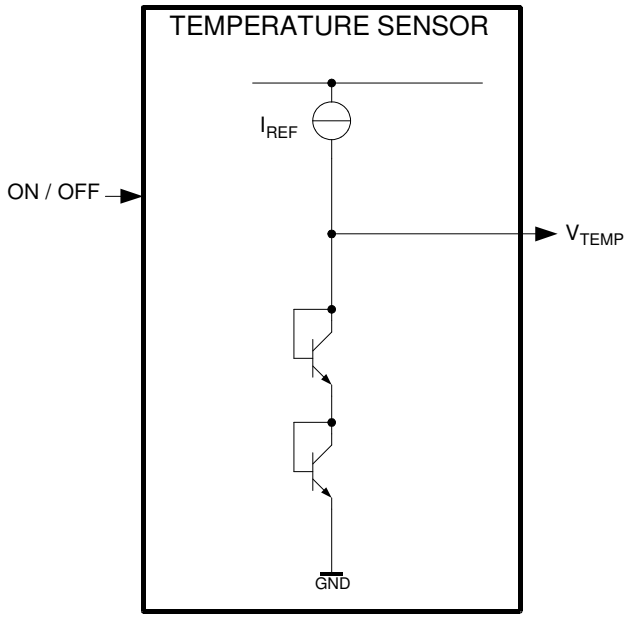


Figure 6.1.4-1: Block Diagram of Temperature Sensor

Functionality of the temperature sensor is to output the temperature dependent voltage V_{TEMP}. V_{TEMP} is realised by supplying two NPN transistor diodes with the current I_{REF}.
At room temperature (25°C) $V_{TEMP}$is in the range defined by $V_{TEMP,25}$. The slope of V_{TEMP} over temperature is given by $SLOPE_{VTEMP}$.
V_{TEMP} can be passed to the ADC via the ADC multiplexer.
The Temperature Sensor is switched on and off according to the actual IC operating mode in order to reduce current consumption in modes, where a temperature measurement is not needed.

6.1.5 Oscillator

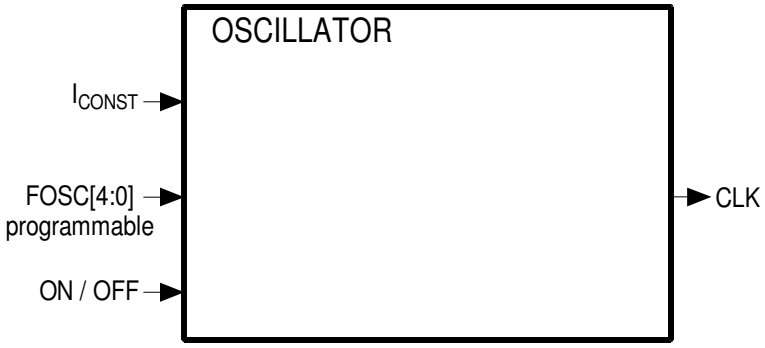


Figure 6.1.5-1: Block Diagram of Oscillator

The oscillator generates the system clock CLK for the Digital Control block. The frequency $F_{CLK,TRIM}$ is defined by:
- internal reference current I_{CONST}
- TRIM Register bits FOSC

During start up of the IC, the register bits FOSC contain default data, the corresponding CLK frequency is according to parameter $F_{CLK,DEF}$.

After start up the calibrated OSC value is readout from OTP and written to register bits FOSC. The corresponding CLK frequency is than according to parameter $F_{CLK,TRIM}$.

The oscillator is switched off only during sleep mode in order to reduce current consumption where CLK is not needed. During start up the oscillator is switched on.

6.1.6 Ambient Light Interface (ALI)

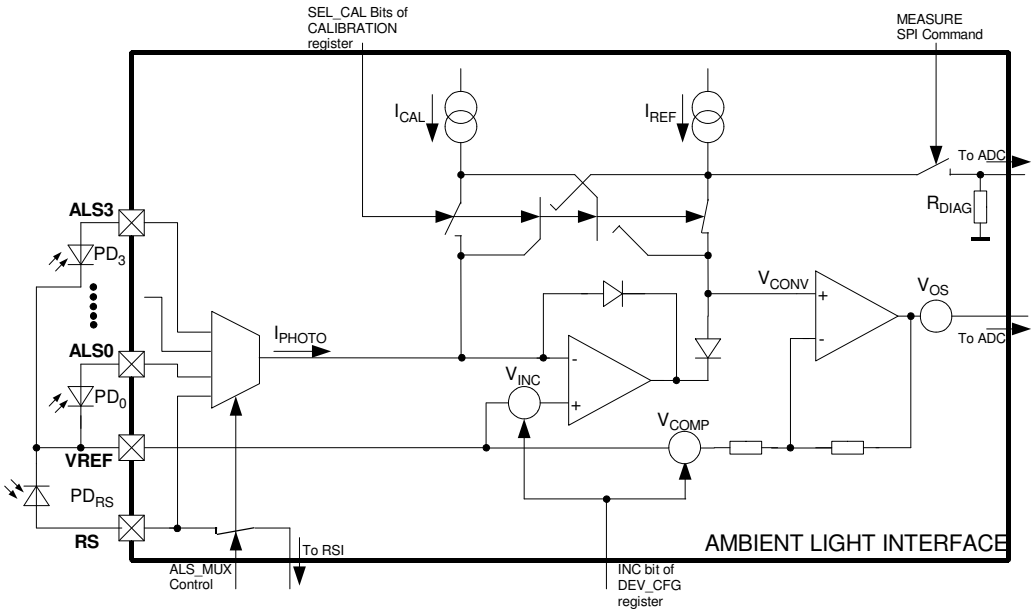


Figure 6.1.6-1: Block Diagram of ALI

The ambient light interface (ALI) is intended to convert the current of an external photo diode into a voltage. This functionality is realized by three functional units:

- input multiplexer
- logarithmic current to voltage converter
- amplifier stage

Input Multiplexer
The input multiplexer of the ALI block is controlled by the internal state machine. According to the chosen channel setting, the current of the external photo diodes, connected to any ALSx or RS pin, is passed via the multiplexer to the input of the logarithmic converter. Any not selected ALSx pin is shorted to VREF. If not selected for light measurement, the current into pin RS is passed to the rain sensor interface.

Logarithmic Converter
The input current I_{PHOTO} is logarithmically converted into a voltage V_{CONV}. Valid input current range of I_{PHOTO} depending on $I_{REF,ALI}$ and amplifier gain is given by parameters $I_{PHOTO,Ix,Gy}$.

V_{INC}
For inputs ALSx and RS an additional systematic offset V_{INC} can be added to the positive input of the logarithmic OP by setting INC via DEV_CFG. This functionality is implemented in order to increase the predictability of ALI's output voltage $V_{ALI,OUT}$ in case of an external short circuit between any ALSx or RS pin, selected for ambient light measurement and any other ALSx pin, RS or VREF.

Without V_{INC} the ALI output voltage can be calculated as follows:

$$V_{ALI,OUT}(I_{PHOTO}) = V_{REF} + G_{ALS,X} \cdot \frac{k \cdot T}{q} \cdot ln\left(\frac{I_{REF,ALI}}{I_{PHOTO}}\right)$$

With activated V_{INC} the output voltage calculation changes to:

$$V_{ALI,OUT}(I_{PHOTO}) = V_{REF} + V_{INC} + G_{ALS,X} \cdot \frac{k \cdot T}{q} \cdot ln\left(\frac{I_{REF,ALI}}{I_{PHOTO}}\right)$$

After measuring the both output voltages and subtraction of V_{INC} from the second one the results should be identical if there is no external short circuit to the selected ALS input. The ALI output voltages can still be identical if the external short circuit has "proper" resistance.

Remark:
As explained above selecting V_{INC} increases the voltage at the corresponding ALS input. Thus the connected photo diode is biased in forward direction what causes a forward current inside the diode. The photo current will be decreased by this forward current. The forward current will increase at higher temperatures.

V_{COMP}
To avoid an amplification of V_{INC} by the amplifier, the compensating voltage source V_{COMP} is implemented. V_{COMP} is activated and deactivated together with V_{INC}. Thus activating V_{INC} increases $V_{ALI,OUT}$ by V_{INC} only and not by V_{INC} multiplied by the amplifier gain. Obviously a mismatch between V_{INC} and V_{COMP} is amplified.

Figure 6.1.6-1 shows a voltage source V_{OS}. This voltage represents the output related offset voltages of the both OP's and in case V_{INC} is activated and a mismatch between V_{INC} and V_{COMP}. The amplifier gain impacts the influence on $V_{ALI,OUT}$.

Pre-charge current with fade-out
A new measure command activates the pre-charge current source $I_{PRECHARGE}$. Charge injection and transitions of switches can load internal nodes far from their operating range. Returning to operating range can take a long time especially when dealing with low currents. $I_{PRECHARGE}$ is sufficiently high to let the logarithmic amplifier return to its operating range fast. After the interval $t_{PRECHARGE}$ the pre-charge current is fade-out smoothly and completely switched off after a second interval $t_{FADEOUT}$ as shown in Figure 6.1.6-2.

The ALI output voltage $V_{ALI,OUT}$ dependent on I_{PHOTO} can be calculated as follows:

$$V_{ALI,OUT}(I_{PHOTO}) = V_{REF} + G_{ALS,X} \cdot \frac{k \cdot T}{q} \cdot ln\left(\frac{I_{REF,ALI}}{I_{PHOTO}}\right)$$

As the input current I_{PHOTO} has to charge several parasitic capacities, a valid measurement result is not available before time $t_{ALI,VAL}$.

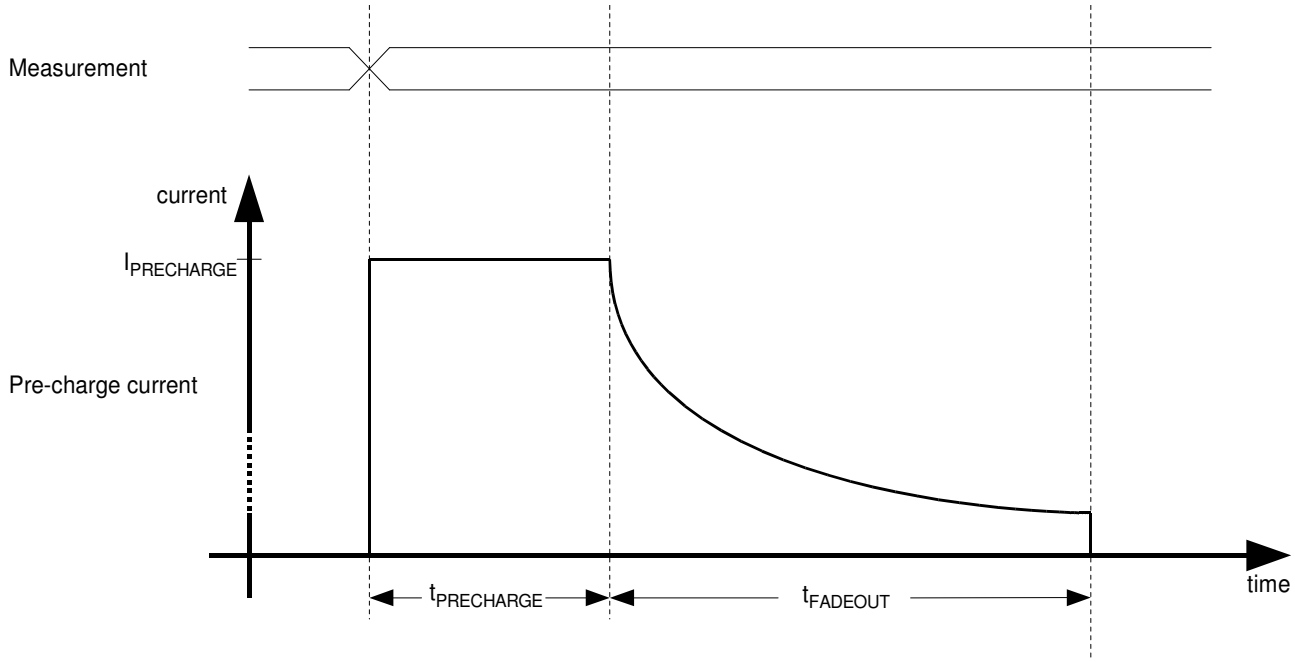


Figure 6.1.6-2: Precharge current

Amplifier Stage
In order to use the full input range of the connected ADC, VCONV is amplified to an appropriate range.

Diagnosis
For diagnosis the reference current can be passed to an internal resistor R_{DIAG}. The corresponding voltages $V_{DIAG,ALI,LO}$ and $V_{DIAG,ALI,HI}$ can be measured via ADC. The measured diagnosis voltages depend on absolute process parameters (due to R_{DIAG}) but show only small variation over temperature. Thus a change of reference current can be easily detected by comparing the actual diagnosis voltage to the corresponding value $V_{DIAG,ALI,X,CAL}$ stored during calibration at room temperature. Tolerances are given by parameters $TOL_{VDIAG,ALI,LO}$ and $TOL_{VDIAG,ALI,HI}$.

$$TOL_{VDIAG,ALI,X} = \frac{V_{DIAG,ALI,X} - V_{DIAG,ALI,X,CAL}}{V_{DIAG,ALI,X,CAL}}$$

Deviations from logarithmic transfer characteristic
So far the transfer characteristic from input current I_{PHOTO} to the measured output value is described by an ideal logarithmic behaviour. But there are deviations from this ideal characteristic:

- For low input currents: ESD protection and Input Multiplexer circuitry cause leakage currents. These leakage currents add to I_{PHOTO} of the photo diode selected for measurement. Thus the measured current is the sum of both. Positive leakage currents are defined as currents flowing into the pad what increases the measured value of I_{PHOTO}, negative leakage currents decrease the measured value as depicted in Figure 6.1.6-3.

Leakage currents are strongly dependent on temperature, thus the leakage currents should be specified for room temperature and high temperature. But as the leakage currents into ALSx pins and RS pin, even at high temperature, are close to the measurement resolution the leakage current is specified over the full temperature range by parameters $I_{LEAK,ALSX}$ and $I_{LEAK,RS}$.

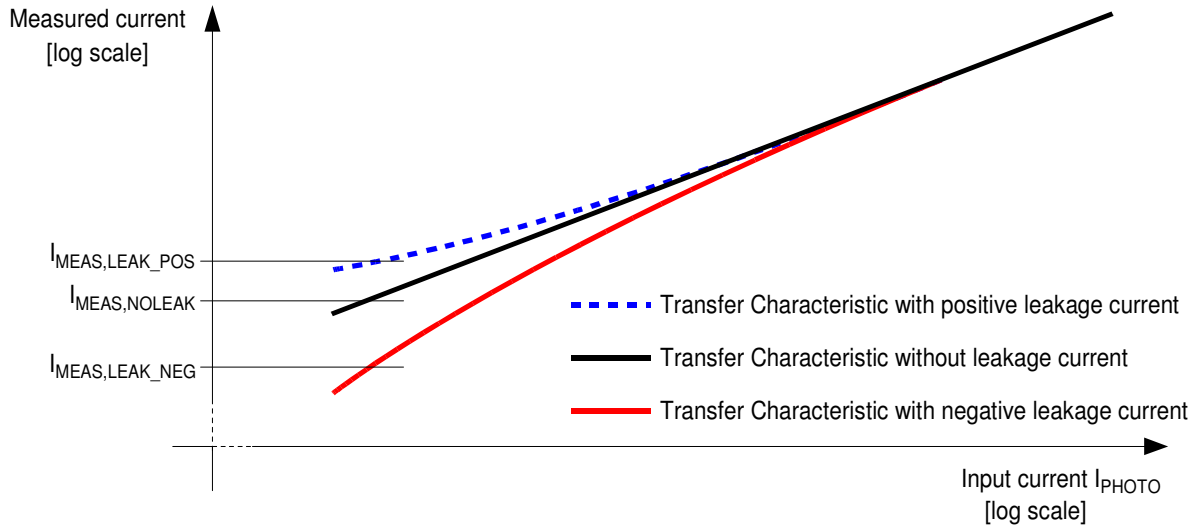


Figure 6.1.6-3: Deviations for low input currents

- For high input currents: The current to voltage characteristic of the Log-Converter diodes is not an ideal logarithmic transfer (e.g. due to intrinsic line resistance). Therefore the measured current is greater than the input current I_{PHOTO}. This deviation increase with increasing input current I_{PHOTO}. So the impact of this deviation can be seen for example on the parameter $I_{MEAS,300u}$.

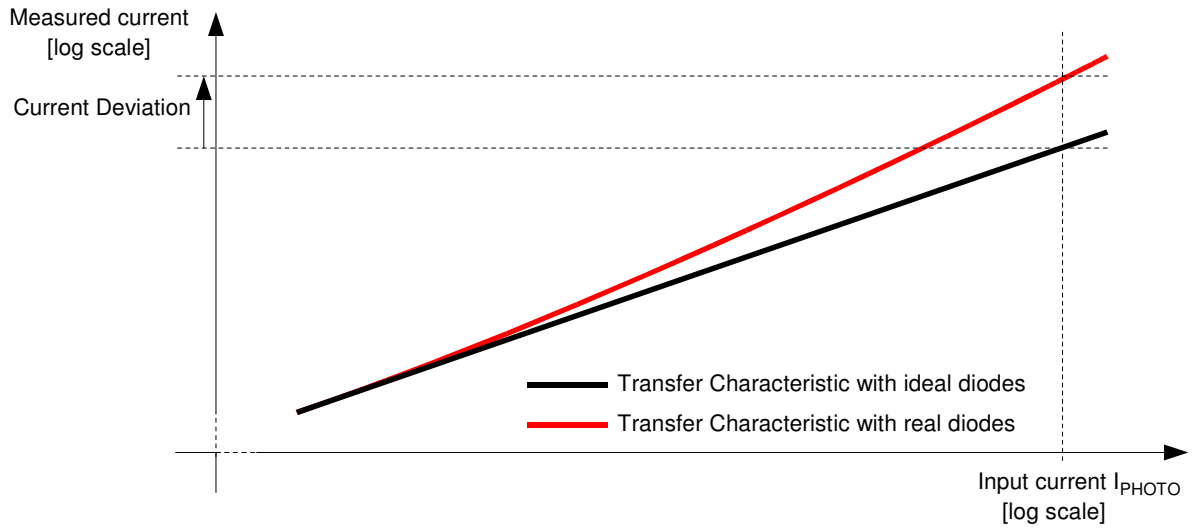


Figure 6.1.6-4: Deviations for high input currents

Calibration
For accurate light measurement the system should be calibrated. The calibration procedure for ALI measurements has to be divided into two categories:
- cyclic calibration during operation of the device
- calibration during end of line test of module

The output voltage should be dependent from the input current like in the following formula:

$$V_{ALI,OUT}(I_{PHOTO}) = V_{REF} + G_{ALS,X} \cdot \frac{k \cdot T}{q} \cdot ln\left(\frac{I_{REF,ALI}}{I_{PHOTO}}\right)$$

correspondingly the photo current can be calculated from:

$$I_{PHOTO} = \frac{I_{REF,ALI}}{exp\left(\frac{V_{ALI,OUT}(I_{PHOTO}) - V_{REF}}{G_{ALS,X} \cdot \frac{kT}{q}}\right)}$$

But the application is intended to measure the ambient light and not I_{PHOTO}. So two other characteristics of the ambient light sensor must be considered in order to get the relation between ambient light and the measured value:

A) the optical path from ambient light to the illuminance of the photo diode and
B) the transfer characteristic of the connected photodiode (illuminance to photo current)

Simplifying both, A and B, to a linear relation, the influence can be described by adding a constant of proportionality. Describing the ambient light by an illuminance IL_{AL} and adding an constant of proportionality $C_{O,PD}$ for the optical path and the photo diode, the above given equations result in:

$$IL_{AL} = \frac{C_{O,PD} \cdot I_{REF,ALI}}{exp\left(\frac{V_{ALI,OUT}(IL_{AL}) - V_{REF}}{G_{ALS,X} \cdot \frac{kT}{q}}\right)}$$

These equations show, that $I_{REF,ALI}$ and $C_{O,PD}$ can be merged to $C_{O,PD,IREF}$. This results in:

$$IL_{AL} = \frac{C_{O,PD,IREF}}{exp\left(\frac{V_{ALI,OUT}(IL_{AL}) - V_{REF}}{G_{ALS,X} \cdot \frac{kT}{q}}\right)}$$

The voltage V_{REF} and the gain coefficient $G_{ALS,X} \cdot \frac{k \cdot T}{q}$ can be extracted by calibration measurements during operation and of course also during the modules end of line test.
The constant of proportionality $C_{O,PD,IREF}$ has to be extracted by a calibration during end of line test of the module as a defined illuminance is required.

Calibration during End of Line Test
In order to extract $C_{O,PD,IREF}$ the equations can be solved to $C_{O,PD,IREF}$.

$$C_{O,PD,IREF} = IL_{AL} \cdot exp\left(\frac{V_{ALI,OUT}(IL_{AL}) - V_{REF}}{G_{ALS,X} \cdot \frac{kT}{q}}\right)$$

With the calibration measurements described below all data is available to calculate the constant of proportionality.

Calibration during operation: gain coefficient
The gain coefficient

$$G_{ALS,X} \cdot \frac{k \cdot T}{q}$$

is proportional to absolute temperature. The actual value can be determined by a calibration measurement during operation.

Selecting a calibration measurement will replace the photo current I_{PHOTO} as ALI input current according to the selected calibration measurement. For such measurement the SEL_CALL bit in the CALIBRATION register has to be set and the channel 5 (IREF) has to be measured. The ALI input current during the calibration measurement will be called I_{CAL} and the related ALI output voltage $V_{ALI,OUT}(I_{CAL})$. Thus the equations given above can be written as:

$$V_{ALI,OUT}(I_{CAL}) = V_{REF} + G_{ALS,X} \cdot \frac{k \cdot T}{q} \cdot ln\left(\frac{I_{REF,ALI}}{I_{CAL}}\right)$$

And solved for the linear coefficient:

$$G_{ALS,X} \cdot \frac{k \cdot T}{q} = \frac{V_{ALI,OUT}(I_{CAL}) - V_{REF}}{ln\left(\frac{I_{REF,ALI}}{I_{CAL}}\right)}$$

The ratio I_{REF}/I_{CALL} is defined in table Table 5.1.5-1 and the determination of V_{REF} is described below.

Calibration during operation: V_{REF}
The reference voltage V_{REF} might also have a slight variation over operating conditions. The actual value can be determined by a calibration measurement during operation. Selecting a calibration measurement will replace the photo current I_{PHOTO} as ALI input current with I_{CAL} like the gain coefficient calibration measurement. V_{REF} can be extracted by two complementary calibration measurements CMA and CMB.

The idea of the complementary measurement is that the reference current I_{REF} and the calibration current I_{CAL} are interchanged: $I_{CAL,B}=I_{REF,A}$ and $I_{REF,B}=I_{CAL,A}$. The corresponding ALI output voltages are $V_{ALI,OUT,CMA}$ and $V_{ALI,OUT,CMB}$:

$$CMA: V_{ALI,OUT,CMA} = V_{REF} + G_{ALS,X} \cdot \frac{k \cdot T}{q} \cdot ln\left(\frac{I_{REF,A}}{I_{CAL,A}}\right)$$
$$CMB: V_{ALI,OUT,CMB} = V_{REF} + G_{ALS,X} \cdot \frac{k \cdot T}{q} \cdot ln\left(\frac{I_{CAL,A}}{I_{REF,A}}\right)$$

Adding up both equations and a following division by 2 :

$$V_{REF} = \frac{V_{ALI,OUT,CMA} + V_{ALI,OUT,CMB}}{2}$$

For the CMA measurement the SEL_CALL bit in the CALIBRATION register must be set and the channel 5 (IREF) has to be measured.

Remark: Due to an implementation error in the M527.05A version the CMB measurement is possible only in test mode. This will be corrected in future version.

6.1.7 Rain Sensor Interface (RSI)

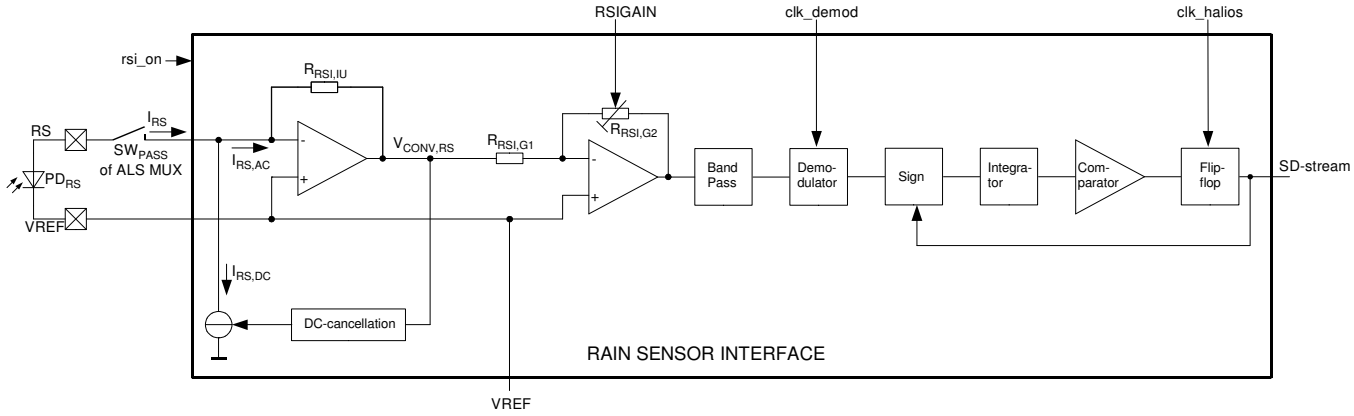


Figure 6.1.7-1: Block Diagram of RSI

The Rain Sensor Interface (RSI) is intended to convert the AC current of the external photo diode connected to pin RS into a voltage. The photo current is passed via ALS-MUX to the RSI.
This functionality is realized by following functional units:

- Current to voltage converter
- DC current cancellation
- Adjustable amplifier stage
- Bandpass filter
- Demodulator
- Sign block
- Integrator
- Comparator
- Flip-flop

Current to Voltage Converter
The input current $I_{RS,AC}$ is linearly converted into a voltage $V_{CONV,RS}$.

DC Current Cancellation
Function of this block is to cancel the DC component $I_{RS,DC}$ of the input photo current I_{RS}. Thus $V_{CONV,RS}$ is fed back via an integrator and a voltage controlled current source.

Adjustable Amplifier Stage
In order to use the full input range of the connected ADC, $V_{CONV,RS}$ is amplified to an appropriate range. By register RSI_CFG1.RSIGAIN, overall gain of the RSI can be set to a value between $G_{RSI,LO}$ and $G_{RSI,HI}$ in N_{GRSI} steps of $G_{RSI,STEP}$.

Bandpass Filter
The bandpass filter is intended to reduce noise.

Demodulator
The demodulator passes the converted input current only during the LED light pulses. The length (integration time) and the phase delay of this conduction period is configurable by the register RSI_CFG3.

Sign block
The demodulated input signal is inverted when the LEDB is active.

Integrator
The light pulses from LEDA are integrated positive and the light pulses from LEDB are integrated negative.

Comparator
The comparator works as an 1 Bit-ADC in a SD-loop.

Flip-flop
The flip-flop synchronize the comparator output with the halios clock and generates therewith the Sigma-Delta stream (SD-stream) output. The SD-stream output decides which LED is active and is also the measurement signal (after digital filtering).

ON and OFF Functionality
The RSI is switched off in sleep mode in order to reduce current consumption.

6.1.8 LED Driver

The two LED drivers for LEDA and LEDB are NMOS current sinks with separately programmable current strength. The current slew rate is limited and a small off current is implemented. The drivers are controlled by the synchronized comparator output from RSI.

The LED drivers are designed to drive up to 4 LEDs per driver. But the max. number of LEDs is dependent from the LED supply voltage and the characteristics of the LEDs. It is important that the voltage at the pins LEDA and LEDB falls not below the minimum value of V_{LEDx} when the driver is activated.

6.1.9 Digital Control

The device operation is controlled with a state-machine that handles user initiated and automatic measurement. A sleep mode is also provided to reduce the power consumption of the device if no measurements are needed.

A state-diagram is given in figure Figure 6.1.9-1.

The state-machine consist of temporary and permanent states. A temporary state is automatically left after a desired action is finished while a permanent state is kept until an external event enforces a state change.

The following subsections describe the relevant details of each state.

State Diagram

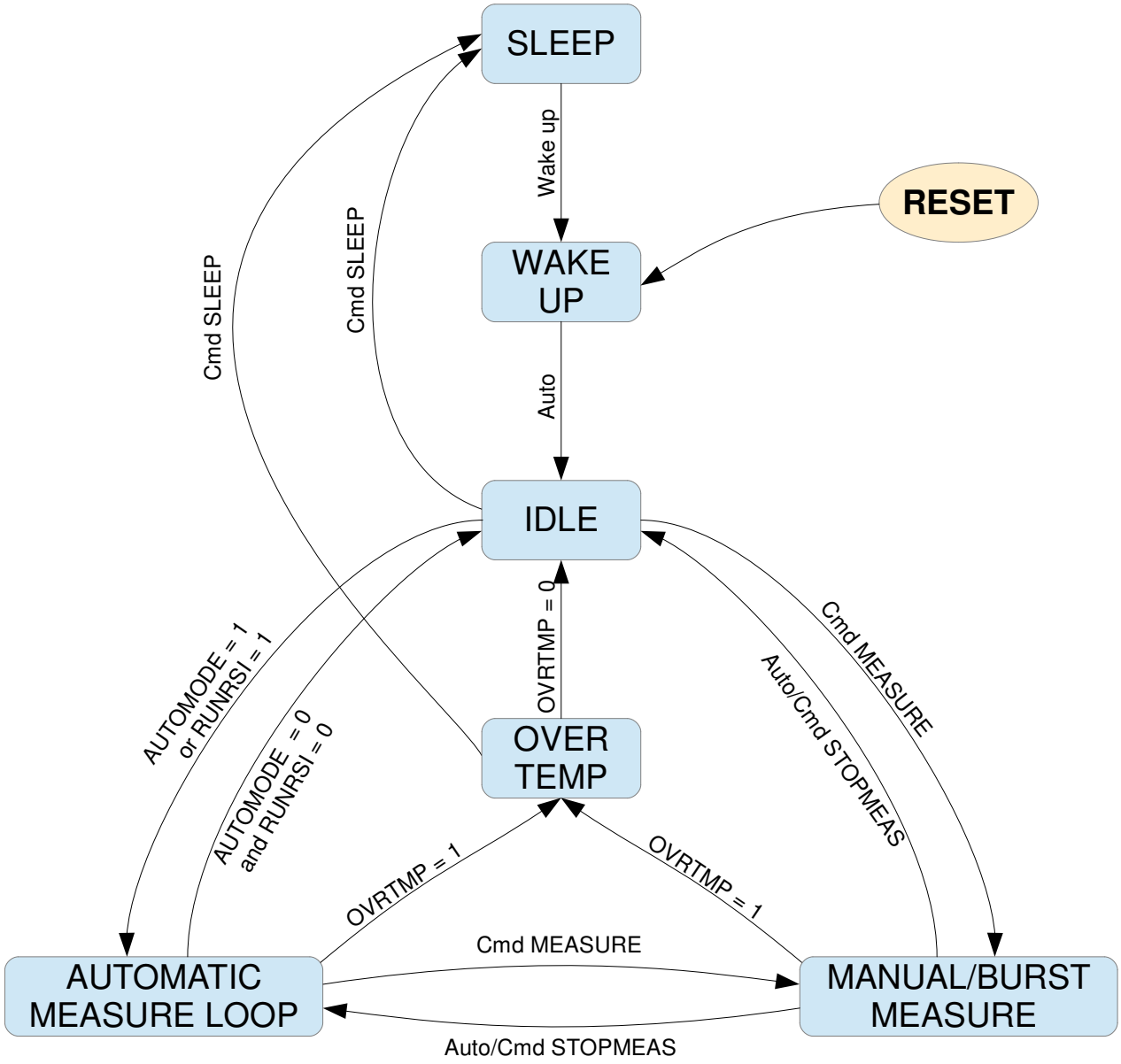


Figure 6.1.9-1: Main state diagram

The device features a digital overtemperature protection that uses the internal temperature sensor and the ALS ADC to monitor the device temperature and watch overtemperature conditions.

The automatic temperature monitoring (FTM = Forced Temperature Measurement) is started automatically when the RSI or ALI measurement loops are started. When the FTM is running a new temperature measurement is requested every 16ms. When a request is pending, the ALS unit executes the temperature measurement at the next available time slot.

If a burst measurement is running, it is interrupted for the FTM measurement without discharging the log amplifier of the selected ALS channel. Hence the settle time of the log amplifier is not extended by the FTM measurement.

6.1.9.1 Wakeup

After power-up or RESET the device reads the trimming values from the OTP and enters the IDLE state.

Table 6.1.9.1-1: WakeUp

Blocks/Function	*Description*
Main Function	Reading the trimming values from the OTP and enters the idle state.
Analog part	OFF
ALI-ADC	OFF
ALI	OFF
RSI-Loop	OFF
LEDs	OFF
Digital control	No access to the registers. All measurements are stopped. Commands are not accepted
Following states	IDLE state

6.1.9.2 Idle Mode

In the IDLE state the device is ready to run but does not execute any measurement. It waits for a new command to execute.

Table 6.1.9.2-1: Idle mode

Blocks/Function	*Description*
Main Function	Wait for new commands.
Analog part	ON
ALI-ADC	OFF
ALI	OFF
RSI-Loop	OFF
LEDs	OFF
Digital control	Full access to the registers. All measurements are stopped. Commands are accepted.
Following states	Manual measurement mode (triggered by the SPI Measure Command) Automatic measurement mode (triggered by setting the AUTOMODE bit in the Mode register) Sleep Mode (triggered by the SPI Sleep Command)

6.1.9.3 Manual/Burst measurement mode

In this state a single measurement or a burst (ongoing repeated) measurement on a selected channel is executed. The result(s) are written into the ADC-value register. In case of a temperature measurement the result is also written into the VTEMP-value register.

When a measurement is requested by the user the measurement is queued as first measurement into the ALS measurement queue. Hence it will become the next ALS measurement to execute. A pending automatic temperature measurement (all 16ms) will be handled in front of the requested measurement anyway.

The BUSY bit in the STATUS register is set when the measurement is queued and cleared when the measurement is finished.

When the BURSTMODE bit is set in the MODE register, the measurement is repeatedly executed on the selected channel without any delay between two consecutive measurements. Averaging, as defined with the MEASAVG bits, still applies. The measurements can be stopped with the STOPMEASURE command via SPI or resetting the BURSTSMODE bit. Automatic temperature measurements are interspersed all 16ms.

Table 6.1.9.3-1: Manual/Burst measurement mode

Blocks/Function	***Description***
Main Function	Manual triggered measurement on a single ALS channel
Analog part	ON
ALI-ADC	ON
ALI	ON when an ALI channel is selected.
RSI-Loop	ON when the MODE.RUNRSI bit is set.
LEDs	ON when the MODE.RUNRSI bit is set.
Digital control	Read access to all result registers. Read and write access to all configuration registers.
Following states	Idle mode (entered after the measures was finished or stopped and automatic measurement mode is not active) Automatic measurement mode when entered from this mode due to a MEASURE command or an automatic temperature measurement Overtemp when a overtemp condition is recognised.

6.1.9.4 Automatic measurement mode

The automatic measurement mode consist of two (mostly) independent measurement loops. The ambient light measurements (ALS) and the rain sensor measurements (RSI).
Both loops are configured and run independent of the other. Synchronizing the measurements is provided by the BLANKRSI bit in the AUTOM_CFG register to provide a better signal to noise ratio, if needed.

The ALS automeasure loop makes repeated measures of all selected channels in the AUTOMCFG register and updates the corresponding data value registers. Each measurement might be the average value according to the value of the AUTOAVG bits in the AVG_CFG register.

The RSI measurement loop makes a rain sensor measurement all 10µs and provides the demodulated result to the RSIVAL register. The loop can be stopped or continued with setting or resetting the HOLDRSI bit in the MODE register.

To prevent overheating an automatic temperature measurement is interspersed every 16 ms and the result is stored in the VTEMP register.

Table 6.1.9.4-1: Automatic measurement mode

Blocks/Function	*Description*
Main Function	Make repeated measures of all selected channels and update the corresponding data value registers. Make a temperature measurement every 16 ms and update the vtemp register.
Analog part	ON
ALS-ADC	ON
ALI	ON
RSI-Loop	ON when the MODE.RUNRSI bit is set.
LEDs	ON when the MODE.RUNRSI bit is set.
Digital control	Read access to all result registers. Read and write acces to all configuration registers.
Following states	Idle mode (triggered by setting the RUNRSI and AUTO-MODE bits in the Mode register to '0') Burst measurement mode (triggered by the SPI measure command) Overtemp when a overtemp condition is recognised.

6.1.9.5 Overtemperature Mode

Overtemperature mode is entered by the device when an overtemperature condition is detected during a measurement.
All running measurements are stopped and no further measurement requests are accepted until the temperature recovers to an acceptable value.

The automatic temperature measurement is executed as long as the overtemperature condition consists.

The OVERTEMP bit in the STATUS register is set and can be cleared if the temperature recovers under the overtemperature threshold value.

Table 6.1.9.5-1: Overtemperature Mode

Blocks/Function	*Description*
Main Function	Keep the device in a save state while the device cools down after switching off huge parts of the device due to an overtemperaure condition.
Analog part	ON
ALI-ADC	ON
ALI	OFF
RSI-Loop	OFF
LEDs	OFF
Digital control	All measurements but the automatic temperature measurement are stopped. No start of measurements is accepted.
Following states	Idle mode when the overtemperature condition is gone.

6.1.9.6 Sleep Mode

The sleep mode is entered using an SPI command to reduce power consumption when no measurements or configurations are made.
It shut down all unused device units including the oscillator and requires new SPI activity for wake-up.

Table 6.1.9.6-1: Sleep mode

Blocks/Function	*Description*
Main Function	Low Power Mode to reduce power consumption when no measurements or configurations are made.
Analog part	OFF
ALI-ADC	OFF
ALI	OFF
RSI-Loop	OFF
LEDs	OFF
Digital control	No access to the device at all. Only the WAKEUP with falling edge of CSB is accepted. All measurements need to be stopped before this state can be entered.
Following states	Leaving sleep mode (WakeUp) returns to the Idle mode.

6.1.9.7 Digital Control Register

The next view sections provide information about the device registers and describe their bits.

Table 6.1.9.7-1: Register Description

Register Name	*Address*	*Description*
STATUS	0	Status register of the device.
MODE	1	Device mode settings.
CALIBRATION	2	Device calibration.
DEV_CFG	3	Device configuration.
RSI_CFG1	4	RSI mode and configuration settings.
RSI_CFG2	5	LEDA/LEDB current sink value.
RSI_CFG3	6	RSI timing settings.
RSI_OUT_THR	7	Threshold value of the RSI threshold comparator.
AUTOM_CFG	8	Automatic measurement configuration.
LOG_EPS	9	Acceptable difference of ADC values while settling the ALI-LOG amp.
AVG_CFG	10	Average exponents for ADC measurements.
RSIVALH	14	Most significant bits of the RSI value.
RSIVALL	15	Least significant bits of the RSI value.
ADCVALH	16	Most significant bits of the ADC value register from the last manual measurement.
ADCVALL	17	Least significant bits of the ADC value register from the last manual measurement.
VTEMPH	18	When "automatic measurement mode" or "rain sensor measurement mode" is active, the most significant bits of the automatic temperature measurement.
VTEMPL	19	When "automatic measurement mode" or "rain sensor measurement mode" is active, the least significant bits of the automatic temperature measurement.

Register Name	Address	Description
ALS0H	20	In "automatic measurement mode" the most significant bits of the ambient light sensor 0 value.
ALS0L	21	In "automatic measurement mode" the least significant bits of the ambient light sensor 0 value.
ALS1H	22	In "automatic measurement mode" the most significant bits of the ambient light sensor 1 value.
ALS1L	23	In "automatic measurement mode" the least significant bits of the ambient light sensor 1 value.
ALS2H	24	In "automatic measurement mode" the most significant bits of the ambient light sensor 2 value.
ALS2L	25	In "automatic measurement mode" the least significant bits of the ambient light sensor 2 value.
ALS3H	26	In "automatic measurement mode" the most significant bits of the ambient light sensor 3 value.
ALS3L	27	In "automatic measurement mode" the least significant bits of the ambient light sensor 3 value.
RSI/ALS4H	28	In "automatic measurement mode" the most significant bits of the rain sensor output value. (Intended for use as fifth ALI channel only)
RSI/ALS4L	29	In "automatic measurement mode" the least significant bits of the rain sensor output value. (Intended for use as fifth ALI channel only)
ICALH	30	In "automatic measurement mode" the most significant bits of the ALI calibration current value.
ICALL	31	In "automatic measurement mode" the least significant bits of the ALI calibration current value.

Table 6.1.9.7-2: Register **STATUS** (0) Status register of the device.

	MSB							LSB
Content	DEVRDY	RST	OVER_TEMP	OVER_VOLTAGE	Reserved[3:1]			BUSY
Reset value	0	1	0	0	0			0
Access	R	R/W	R/W	R/W	R			R
Bit Description	**DEVRDY** : This bit signals that the device is out of the initialisation phase and ready to work. Unless this bit is set AUTOMODE and RUNRSI bits are stored but not executed. Only READ- & WRITE commands are accepted while DEVRDY is not set. **RST** : This bit is set always after a system reset and also after power up. The bit can be cleared by writing a '1'. **OVER_TEMP** : Over Temperature occurred. The bit can be cleared by writing a '1' when the over-temp condition has vanished. **OVER_VOLTAGE** : Over Voltage occurred. The bit can be cleared by writing a '1'. **Reserved[3:1]** : Reserved. Read as 0. **BUSY** : When the busy bit is set, the device processes a pending measure. In the manual measurement mode the bit is reseted when the measurement is finished and the result of the measurement is available.							

Table 6.1.9.7-3: Register **MODE** (1) Device mode settings.

	MSB							***LSB***
Content	HOLDRSI	RUNRSI	AUTO-MODE	BURST-MODE	Reserved	WSFCT[2:0]		
Reset value	0	0	0	0	0	0		
Access	R/W	R/W	R/W	R/W	R	R/W		
Bit Description	**HOLDRSI** : Writing a '1' to this bit disables the LEDs and pause the HALIOS rain sensor measurement. In contrast to clearing the RUNRSI bit, setting HOLDRSI does not reset the low- and highpass filter states. Hence the filter does not need to full settle when the RSI measurement is reinvoced by clearing HOLDRSI later. **RUNRSI** : Writing a '1' to this bit enables the LEDs and starts the HALIOS rain sensor loop. Writing a '0' to this bit disables the LEDs, switches off the HALIOS rain sensor measurement and resets the current low- and highpass filter states. Note that manual and automatic measurement of the RSI/ALS4 channel is not possible if RUNRSI is set. Accordingly RUNRSI can not be set if a manual or automatic measurement of the RSI/ALS4 channel is running (or possible). **AUTOMODE** : Writing a '1' to this bit starts the automatic measurement mode. Writing a '0' to this bit stops the automatic measurement mode. Note that automatic measurement of the RSI/ALS4 channel is not possible if RUNRSI is set. **BURSTMODE** : Writing a '1' to this bit forces MEASURE commands to run in burst mode. **Reserved** : Reserved. Read as zero. **WSFCT[2:0]** : Function of the WS output pin: b000: No output b001: Sigma-Delta stream output (SD-stream) of RSI (additional Data Available Pulse at pin MISO) b010: Only for production test: output of RSI comparator b011: Output of the digital threshold comparator b100: Output pulse if a new value from RSI is available b101: Output pulse if a new measurement value from ALI is available b110: No output (stored as b000) b111: Only for production test: output equals input of pin TMODE							

Table 6.1.9.7-4: Register **CALIBRATION** (2) Device calibration.

	MSB							***LSB***
Content	Reserved[7:2]						SEL_CALH	SEL_CALL
Reset value	0						0	0
Access	R						R/W	R/W
Bit Description	**Reserved[7:2]** : Reserved. Read as 0. **SEL_CALH** : Only for production test. **SEL_CALL** : Selects the ICAL calibration current as input of the ALI-LOG amplifier (described in chapter 6.1.6).							

Table 6.1.9.7-5: Register **DEV_CFG** (3) Device configuration.

	MSB							***LSB***
Content	Reserved[7:3]					INC	NOPAR-ITY	SELDRV
Reset value	0					0	0	1
Access	R					R/W	R/W	R/W
Bit Description	**INC** : Systematic offset of ALI for short circuit detection. **NOPARITY** : Writing a '1' to this bit disables the processing of the TX parity bit and the sending of the status byte (including the RX parity bit) after sending a data word to the SPI master. Changes to this bit become valid at the end of the transaction (rising edge of CSB) that changes the bit. **SELDRV** : Select pad driving capability for MISO and WS: b0: less drive capability b1: normal drive capability							

Table 6.1.9.7-6: Register **RSI_CFG1** (4) RSI mode and configuration settings.

	MSB							***LSB***
Content	RSIGAIN[7:4]				Reserved	QUAD_SPULS	BYPASS_HP	RSI_MODE
Reset value	0				0	0	0	0
Access	R/W				R	R/W	R/W	R/W
Bit Description	**RSIGAIN[7:4]** : Gain of the RSI input amplifier in 2.8 dB steps. **Reserved** : Reserved. Read as 0. **QUAD_SPULS** : When set, the update frequency of the RSI samples in the RSIVAL register is increased by (oversampling-)factor 4. However, this does not change the lowpass filter frequency. **BYPASS_HP** : Bypass the highpass filter. b0: no bypass b1: bypass **RSI_MODE** : RSI timing mode. b0: default mode b1: alternatively mode Note that RSI_MODE can not be changed if MODE.RUNRSI is set.							

Table 6.1.9.7-7: Register **RSI_CFG2** (5) LEDA/LEDB current sink value.

	MSB							***LSB***
Content	IW_LEDB[7:4]				IW_LEDA[3:0]			
Reset value	0				0			
Access	R/W				R/W			
Bit Description	**IW_LEDB[7:4]** : Work current sink value for LEDB in 2.5mA steps. b0000: 2.5mA b0001: 5.0mA ... b1111: 40.0mA **IW_LEDA[3:0]** : Work current sink value for LEDA in 2.5mA steps. b0000: 2.5mA b0001: 5.0mA ... b1111: 40.0mA							

Table 6.1.9.7-8: Register **RSI_CFG3** (6) RSI timing settings.

	MSB							***LSB***
Content	PHASE_DELAY[3:0]				SAMPLE_ TIME	FREQ_SHIFT[2:0]		
Reset value	0				0	0		
Access	R/W				R/W	R/W		
Bit Description	**PHASE_DELAY[3:0]** : Phase delay of the integration phase of RSI in 125ns steps (demodulator at chapter 6.1.7). b0000: min. phase delay ... b1111: max. phase delay **SAMPLE_TIME** : Length of integration phase of RSI (demodulator at chapter 6.1.7) b0: 3 us b1: 2 us **FREQ_SHIFT[2:0]** : RSI modulator periode (Halios periode) [us]: b000: 10,0 b001: 10,25 ... b111: 11,75							

Table 6.1.9.7-9: Register **RSI_OUT_THR** (7) Threshold value of the RSI threshold comparator.

	MSB							***LSB***
Content	THR_LVL[7:0]							
Reset value	0							
Access	R/W							
Bit Description	**THR_LVL[7:0]** : Threshold value of the RSI threshold comparator. The 8-bit value is extended to a 10 bit signed value by right and left padding b0 and then compared with the output of the bandpass filtered RSI bit stream (RSIVAL). If the absolute value of RSIVAL is greater than the extended THR_LVL the comparator outputs a logic '1', otherwise a logic '0'. The output is visible at WS (MODE.WSFCT: 011b)							

Table 6.1.9.7-10: Register **AUTOM_CFG** (8) Automatic measurement configuration.

	MSB							***LSB***
Content	BLANKRSI	Reserved	ICAL	RSIALS4	ALS3	ALS2	ALS1	ALS0
Reset value	0	0	0	0	0	0	0	0
Access	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
Bit Description	**BLANKRSI** : Experimental feature: This bit is only useful when RSI and ALS (automeasure/MEASURE-cmd) measurements are made in parallel. When this bit is set, RSI measurement is suspended while the ALI ADC is sampling to ensure a better signal to noise ratio. When this bit is cleared (default) RSI and ALI measurements runs complete independent. **Reserved** : Reserved. Read as zero. **ICAL** : When set the ALI calibration current is measured in the automatic measurement loop. When cleared this measurement is skipped. Note: To measure the ALI calibration current additional settings (calibration register) must be made. **RSIALS4** : When set the rain sensor diode is measured in the automatic measurement loop. This is intended for using the rain sensor input as fifth ALI channel. Setting this bit clears the RUNRSI bit in the MODE register and the LEDs are permanent switched off. When cleared the measurement is skipped. **ALS3** : When set the ambient light sensor 3 diode is measured in the automatic measurement loop. When cleared this measurement is skipped. **ALS2** : When set the ambient light sensor 2 diode is measured in the automatic measurement loop. When cleared this measurement is skipped. **ALS1** : When set the ambient light sensor 1 diode is measured in the automatic measurement loop. When cleared this measurement is skipped. **ALS0** : When set the ambient light sensor 3 diode is measured in the automatic measurement loop. When cleared this measurement is skipped.							

Table 6.1.9.7-11: Register **LOG_EPS** (9) Acceptable difference of ADC values while settling the ALI-LOG amp.

	MSB							***LSB***
Content	LOG_EPS[7:0]							
Reset value	0							
Access	R/W							
Bit Description	**LOG_EPS[7:0]** : While the ALI-LOG amplifier is settling the end of the settling phase is assumed when two consecutive measurements with the ADC have a difference smaller than LOG_EPS. These automatic settling of the ALI-LOG amplifier is disabled at burst mode.							

Table 6.1.9.7-12: Register **AVG_CFG** (10) Average exponents for ADC measurements.

	MSB							***LSB***
Content	TEMPAVG[7:6]		MEASAVG[5:3]			AUTOAVG[2:0]		
Reset value	0		0			0		
Access	R/W		R/W			R/W		
Bit Description	**TEMPAVG[7:6]** : Exponent of the number of ADC values averaged when an auto. temperature measurement is executed. The number of ADC values averaged is given by $n = 2^{TEMPAVG}$. The maximum number for TEMPAVG is 3 (binary "11"). This results in an averaging of 8 ADC values. **MEASAVG[5:3]** : Exponent of the number of ADC values averaged when a MEASUREMENT (SPI) command is executed. The number of ADC values averaged is given by $n = 2^{MEASAVG}$. The maximum number for MEASAVG is 4 (binary "100"). This results in an averaging of 16 ADC values. When a value greater than 4 is written to MEASAVG it will be clipped down to 4. **AUTOAVG[2:0]** : Exponent of the number of ADC values averaged in the "automatic measurement mode" The number of ADC values averaged is given by $n = 2^{AUTOAVG}$. The maximum number for AUTOAVG is 4 (binary "100"). This results in an averaging of 16 ADC values. When a value greater than 4 is written to AUTOAVG it will be clipped down to 4.							

Table 6.1.9.7-13: Register **RSIVALH** (14) Most significant bits of the RSI value.

	MSB							***LSB***
Content	ERROR	INVALID	Reserved[5:2]				RSIVAL[9:8]	
Reset value	1	0	0				0	
Access	R	R	R				R	
Bit Description	**ERROR** : This bit is set always after a system reset (also after power up) or if Over Temperature or Over Voltage occurred. **INVALID** : Value RSIVAL is invalid. **Reserved[5:2]** : Reserved. Read as 0. **RSIVAL[9:8]** : Most significant bits of the RSI value. Note: RSIVAL[9:0] is a signed number in two's complement format.							

Table 6.1.9.7-14: Register **RSIVALL** (15) Least significant bits of the RSI value.

	MSB							***LSB***
Content	RSIVAL[7:0]							
Reset value	0							
Access	R							
Bit Description	**RSIVAL[7:0]** : Least significant bits of the RSI value. Note: RSIVAL[9:0] is a signed number in two's complement format.							

Table 6.1.9.7-15: Register **ADCVALH** (16) Most significant bits of the ADC value register from the last manual measurement.

	MSB							***LSB***
Content	ERROR	CHN_INVALID	Reserved[5:2]				ADCVAL[9:8]	
Reset value	1	0	0				0	
Access	R	R	R				R	
Bit Description	**ERROR** : This bit is set always after a system reset (also after power up) or if Over Temperature or Over Voltage occurred. **CHN_INVALID** : Bit is set if the measured Channel is not stable with respect of the selected LOG_EPS value. **Reserved[5:2]** : Reserved. Read as 0. **ADCVAL[9:8]** : Most significant bits of the ADC value							

Table 6.1.9.7-16: Register **ADCVALL** (17) Least significant bits of the ADC value register from the last manual measurement.

	MSB							***LSB***
Content	ADCVAL[7:0]							
Reset value	0							
Access	R							
Bit Description	**ADCVAL[7:0]** : Least significant bits of the ADC value							

Table 6.1.9.7-17: Register **VTEMPH** (18) When "automatic measurement mode" or "rain sensor measurement mode" is active, the most significant bits of the automatic temperature measurement.

	MSB							***LSB***
Content	ERROR	Reserved[6:2]					VTEMP[9:8]	
Reset value	1	0					11	
Access	R	R					R	
Bit Description	**ERROR** : This bit is set always after a system reset (also after power up) or if Over Temperature or Over Voltage occurred. **Reserved[6:2]** : Reserved. Read as 0. **VTEMP[9:8]** : Most significant bits of the VTEMP value							

Table 6.1.9.7-18: Register **VTEMPL** (19) When "automatic measurement mode" or "rain sensor measurement mode" is active, the least significant bits of the automatic temperature measurement.

	MSB							***LSB***
Content	VTEMP[7:0]							
Reset value	11111111							
Access	R							
Bit Description	**VTEMP[7:0]** : Least significant bits of the VTEMP value							

Table 6.1.9.7-19: Register **ALS0H** (20) In "automatic measurement mode" the most significant bits of the ambient light sensor 0 value.

	MSB							***LSB***
Content	ERROR	CHN_INVALID	Reserved[5:2]				ALS0[9:8]	
Reset value	1	0	0				0	
Access	R	R	R				R	
Bit Description	**ERROR** : This bit is set always after a system reset (also after power up) or if Over Temperature or Over Voltage occurred. **CHN_INVALID** : Bit is set if the Channel is not stable with respect of the selected LOG_EPS value. **Reserved[5:2]** : Reserved. Read as 0. **ALS0[9:8]** : Most significant bits of ambient light sensor 0							

Table 6.1.9.7-20: Register **ALS0L** (21) In "automatic measurement mode" the least significant bits of the ambient light sensor 0 value.

	MSB							***LSB***
Content	ALS1[7:0]							
Reset value	0							
Access	R							
Bit Description	**ALS1[7:0]** : Least significant bits of ambient light sensor 0							

Table 6.1.9.7-21: Register **ALS1H** (22) In "automatic measurement mode" the most significant bits of the ambient light sensor 1 value.

	MSB							***LSB***
Content	ERROR	CHN_INVALID	Reserved[5:2]				ALS1[9:8]	
Reset value	1	0	0				0	
Access	R	R	R				R	
Bit Description	**ERROR** : This bit is set always after a system reset (also after power up) or if Over Temperature or Over Voltage occurred. **CHN_INVALID** : Bit is set if the Channel is not stable with respect of the selected LOG_EPS value. **ALS1[9:8]** : Most significant bits of ambient light sensor 1							

Table 6.1.9.7-22: Register **ALS1L** (23) In "automatic measurement mode" the least significant bits of the ambient light sensor 1 value.

	MSB							***LSB***
Content	ALS2[7:0]							
Reset value	0							
Access	R							
Bit Description	**ALS2[7:0]** : Least significant bits of ambient light sensor 1							

Table 6.1.9.7-23: Register **ALS2H** (24) In "automatic measurement mode" the most significant bits of the ambient light sensor 2 value.

	MSB							***LSB***
Content	ERROR	CHN_INVALID	Reserved[5:2]				ALS2[9:8]	
Reset value	1	0	0				0	
Access	R	R	R				R	
Bit Description	**ERROR** : This bit is set always after a system reset (also after power up) or if Over Temperature or Over Voltage occurred. **CHN_INVALID** : Bit is set if the Channel is not stable with respect of the selected LOG_EPS value. **Reserved[5:2]** : Reserved. Read as 0. **ALS2[9:8]** : Most significant bits of ambient light sensor 2							

Table 6.1.9.7-24: Register **ALS2L** (25) In "automatic measurement mode" the least significant bits of the ambient light sensor 2 value.

	MSB							***LSB***
Content	ALS2[7:0]							
Reset value	0							
Access	R							
Bit Description	**ALS2[7:0]** : Least significant bits of ambient light sensor 2							

Table 6.1.9.7-25: Register **ALS3H** (26) In "automatic measurement mode" the most significant bits of the ambient light sensor 3 value.

	MSB							***LSB***
Content	ERROR	CHN_INVALD	Reserved[5:2]				ALS3[9:8]	
Reset value	1	0	0				0	
Access	R	R	R				R	
Bit Description	**ERROR** : This bit is set always after a system reset (also after power up) or if Over Temperature or Over Voltage occurred. **CHN_INVALD** : Bit is set if the Channel is not stable with respect of the selected LOG_EPS value. **Reserved[5:2]** : Reserved. Read as 0. **ALS3[9:8]** : Most significant bits of ambient light sensor 3							

Table 6.1.9.7-26: Register **ALS3L** (27) In "automatic measurement mode" the least significant bits of the ambient light sensor 3 value.

	MSB							***LSB***
Content	ALS3[7:0]							
Reset value	0							
Access	R							
Bit Description	**ALS3[7:0]** : Least significant bits of ambient light sensor 3							

Table 6.1.9.7-27: Register **RSI/ALS4H** (28) In "automatic measurement mode" the most significant bits of the rain sensor output value.(Intended for use as fifth ALI channel only)

	MSB							***LSB***
Content	ERROR	CHN_INVALID	Reserved[5:2]				ALS4[9:8]	
Reset value	1	0	O				0	
Access	R	R	R				R	
Bit Description	**ERROR** : This bit is set always after a system reset (also after power up) or if Over Temperature or Over Voltage occurred. **CHN_INVALID** : Bit is set if the Channel is not stable with respect of the selected LOG_EPS value. **Reserved[5:2]** : Reserved. Read as 0. **ALS4[9:8]** : Most significant bits of ambient light sensor 4							

Table 6.1.9.7-28: Register **RSI/ALS4L** (29) In "automatic measurement mode" the least significant bits of the rain sensor output value.(Intended for use as fifth ALI channel only)

	MSB							***LSB***
Content	ALS4[7:0]							
Reset value	0							
Access	R							
Bit Description	**ALS4[7:0]** : Least significant bits of ambient light sensor 4							

Table 6.1.9.7-29: Register **ICALH** (30) In "automatic measurement mode" the most significant bits of the ALI calibration current value.

	MSB							***LSB***
Content	ERROR	CHN_INVALID	Reserved[5:2]				ICAL[9:8]	
Reset value	1	0	0				0	
Access	R	R	R				R	
Bit Description	**ERROR** : This bit is set always after a system reset (also after power up) or if Over Temperature or Over Voltage occurred. **CHN_INVALID** : Bit is set if the Channel is not stable with respect of the selected LOG_EPS value. **Reserved[5:2]** : Reserved. Read as 0. **ICAL[9:8]** : Most significant bits of the ICAL value							

Table 6.1.9.7-30: Register **ICALL** (31) In "automatic measurement mode" the least significant bits of the ALI calibration current value.

	MSB							***LSB***
Content	ICAL[7:0]							
Reset value	0							
Access	R							
Bit Description	**ICAL[7:0]** : Least significant bits of the ICAL value							

6.1.10 Digital Signal Processing

The digital signal processing of the device consists of two independent but loosely synchronized subsystems, the HALIOS based rain sensor measurement subsystem (RSI) and the ADC based ambient light measurement subsystem (ALS). The later also provides measurement of the internal temperature sensor and internal current reference.

Both subsystems can be enabled independently and run almost independent of each other. The RSI subsystem makes measurements (LED pulses) with a frequency of $f_{RSI,MOD}$ while the ALS subsystem in AUTOMODE measures the selected channels in a $t_{ALI,AUTOM}$ timing intervals. Note that a channel measurement can consist of more than one ADC measurement due to averaging.

To reduce disturbances the ADC measurements can be interlaced with LED stimuli of the RSI measurement subsystem using the BLANKRSI bit in the AUTOM_CFG register. This means that ALS measurements are not started parallel to a RSI measurement but are delayed until the actual RSI LED pulse is finished.

Since the ALS input stage may need to settle, it is possible that an ALS measurement takes longer than the time between two consecutive RSI measurements. When BLANKRSI is set then the intersected RSI measurements are skipped.

In extreme situations (i.e. maximum current differences between successive channel measurements) it my be possible that the settling time becomes longer than $t_{ALI,AUTOM}$ (refer $t_{ALI,VALID}$). Then the next ALI channel measurement is delayed to the next $t_{ALI,AUTOM}$ interval time.

When RSI measurement is not selected at all, then no LED stimuli signals are generated. Nevertheless the ADC measurements keep the same timing intervals as when RSI measurements are taken.

For more information on ADC averaging, see chapter 6.1.10.2.

6.1.10.1 Rain sensor data processing

The main subsystem is a HALIOS based rain sensor detection. When active, the subsystem generates stimuli pulses for two LED's as described in Chapter 6.1.7. The received light is used as the input signal for the HALIOS loop.

An overview picture of the RSI subsystem (without SPI interface) is shown in Figure 6.1.10.1-1.

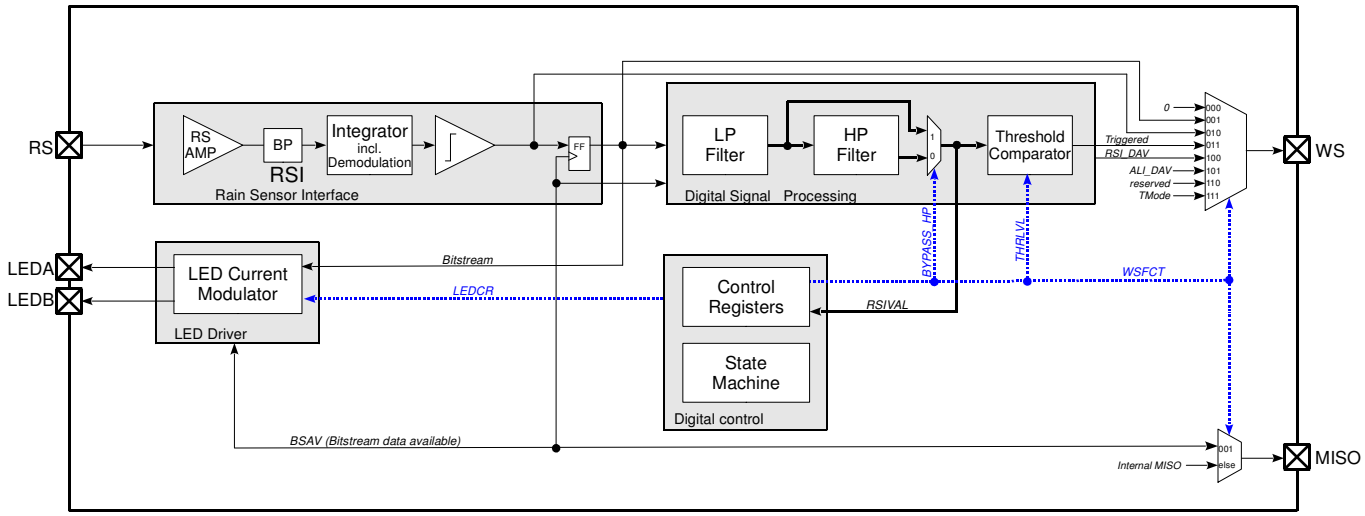


Figure 6.1.10.1-1: The RSI measurement unit

The output of the HALIOS loop is a bit stream that corresponds to the amount of received light reflection of the two LED's.
The bit stream is used to select which of the two LEDs is fired next.

To roughly compensate differences in the common reflection received from the two LED's, the sink current of the LED's can be adjusted in 16 steps for each LED using the RSI_CFG2 register.

Then the bit stream from the HALIOS loop is bandpass-filtered to reconstruct a measure of the received light energy of the LED pulses. This information is stored in the RSIVAL register for further processing.

The output of the bandpass filter (RSIBPO) is fed into a threshold comparator. The threshold level of the comparator can be programmed using the 8-bit THR_LVL value in the RSI_OUT_THR register.
Since the RSIBPO has a 10 bit width, THR_LVL is extended by left- & right-padding a binary zero.

If the RSIBPO value is greater than the extended THR_LVL value, the comparator outputs a logic '1', otherwise a logic '0' The result of the comparison can be switched to the WS pin using the MODE register for further processing.

6.1.10.2 ADC based measurement

The second subsystem is an ADC based measurement system for up to five ambient light sensors, an integrated temperature sensor and an integrated reference voltage.
ADC based measurements can be done in two different flavours, "automatic measurement mode" and "manual measurement mode".

An overview picture of the ALS subsystem (without SPI interface) is shown in figure Figure 6.1.10.2-1.

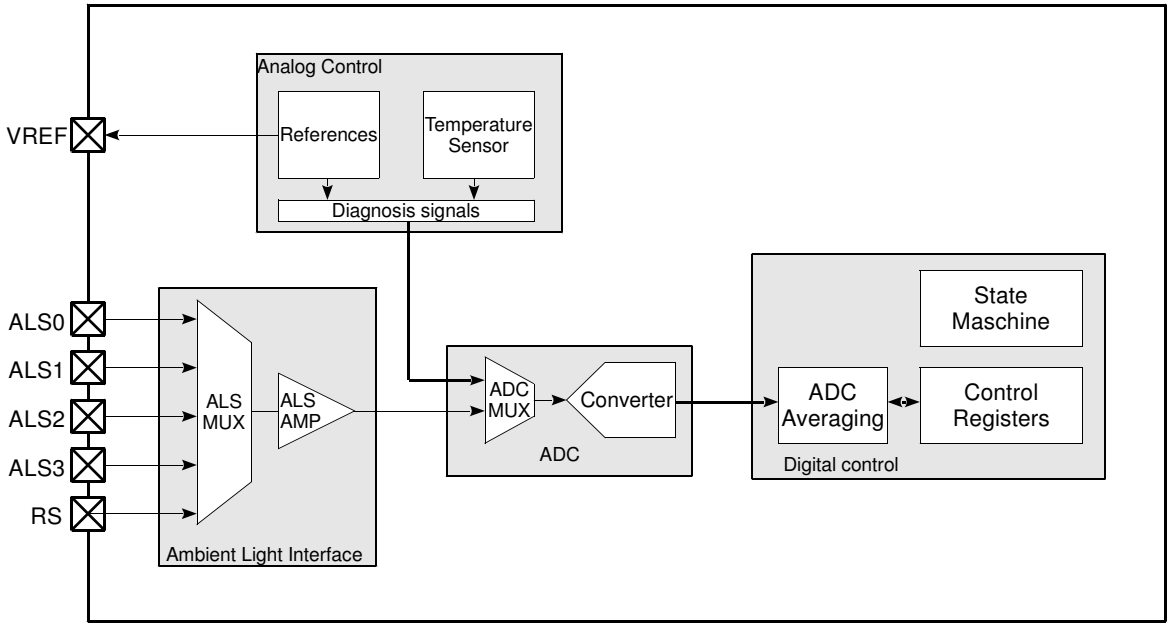


Figure 6.1.10.2-1: The ADC measurement unit

In the **automatic measurement mode** the device measures a predefined set of ADC channels periodically. The channels that should be measured are set in the AUTOM_CFG register.

To reduce noise there is the possibility to automatically average a number of measures before providing the result to the user. The number of averages can be set using the AVGEXP[1:0] bits in the AVG_CFG register.

The result of the measurements are provided in the corresponding registers:

- ALS0-3 - for the ambient light sensors 0-3
- RSI/ALI4 - For the rain sensor. This channel can also be used as fifth ambient light sensor.
- ICAL - for the internal ALI calibration current
- VTEMP - for the internal temperature sensor

The RSI/ALI4 channel is the device input of the rain sensor, measured using the ALI ADC. This channel is useful when a fifth ALI sensor is required and no rain sensor interface is needed.
Selecting this channel for automatic or manual measurement is not possible, when the rain sensor interface is switched on.
Accordingly the RUNRSI bit can not be set when this channel is used for automatic or manual measurement.

In the **manual measurement mode** the user can initialize a one-time measurement with the command MEASURE.

MEASURE takes the channel number as parameter. The applied average is set using the MEASAVG bits in the AVG_CFG register. Note that the number of averages is independent from the value set using the AUTOAVG bits in the same register to allow flexible "single shot" measurements.

With the MEASURE command there are more channels available as in the AUTOMEASURE mode. Refer to table Table 6.1.11.2-2 for a complete list of available channels.

In both modes averaging is done by repeated measurement of a particular channel, before the next channel is processed. The averaged value for each channel is calculated by:

$$avg_{channel} = \frac{1}{N} \cdot \sum_{i=1}^{N} < channel\ \ value\ \ i >$$

with

$$N = 2^{expreg}.$$

The expreg is either TEMPAVG, MEASAVG or AUTOAVG, depending of the executed measurement. These three average exponents can be set in the AVG_CFG register.

Note that this is not a moving average since the intention of this operation is not low pass filtering, but noise reduction.

Since manual measurements are synchronized with running auto-measurements they may not execute immediately. A running manual measure is indicated by the BUSY flag in the status register. When doing a measure in the "manual measurement mode" this flag should be checked to determine if the requested measure was finished.

When the manual measurement is finished the result is available in the ADCVALH/ADCVALL register pair.

A special case of the MEASURE command can be invoked using the **BURSTMODE** bit in the MODE register.

When this bit is set and a MEASURE command is send to the device, a running AUTOMEASURE is interrupted and the MEASURE command is executed repeatedly without any delay between consecutive measures.
The result is available in the ADCVALH/ADCVALL register pair.

This repeated measure can be stopped by either clearing the BURSTMODE bit in the MODE register or by sending a STOPMEAS command to the device. An interrupted AUTOMEASE will be resumed.

6.1.11 Serial Peripheral Interface (SPI)

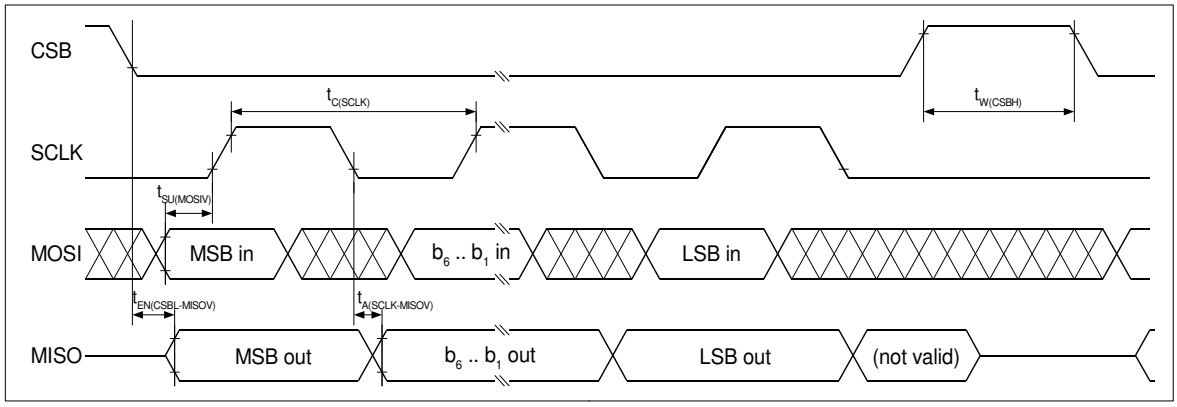


Figure 6.1.11-1: SPI Timing Diagram

The SPI (Serial Peripheral Interface) provides access to the complete control of the device.

6.1.11.1 SPI Format

This chapter gives detailed information about the different command available for the device.

The device supports 3-wire and 4-wire SPI communication. When using 3-wire SPI the CSB signal must be tied to digital ground. No further precaution is needed.
Since CSB is also used for wake-up the device from sleep mode there is no usable sleep mode available with 3-wire SPI. Moreover, since the device can't detect if the CSB pin is used, there is no way to protect the device from executing a SLEEP command accidently send by the SPI master.
Hence 3-wire SPI is not recommended and should be seen as last resort solution when pin count at the SPI master becomes a serious issue.

In this chapter all examples are shown for 4-wire SPI.
On 4-wire SPI a communication cycle starts with a falling edge on CSB. The communication cycle ends with a rising edge on CSB. This sets the MISO output to 3-State and cleans-up the internal SPI state. Processing of more than one transaction in a communication cycle is possible.

Data is transmitted with most significant bit first (MSB).

All communication is made in form of transactions. The SPI works as a slave only. It never initiates a communication cycle. Hence all transaction starts by the SPI master, sending a sequence of bytes to the device.

As first byte of a transaction a command is expected by the device. A list of available commands is given in chapter 6.1.11.2. Depending on the command a data byte is expected as second byte.

Finally the device expects a byte containing a parity bit as MSB. All other bits in this byte are ignored.

The device verifies the received command and data against the parity bit. If the total number of logical ones is not odd, the command is assumed to be corrupted. In this case the device will set the ECS bit in the status byte and does not execute the command.

The parity mechanism can be disabled by setting the NOPARITY bit in the MODE register (see chapter 6.1.9.7). When NOPARITY is set the whole last byte is ignored and the command is always executed (assuming no further errors occur).

With NOPARITY set the ECS bit in the status byte is always set, to signal that no successful parity check was done.

- NOTE: For reading data from the device the master doesn't need to provide the parity byte at all. This is due to the fact that reading data can't provide any harm to the device state. Hence the device handle all read commands in the same way as when the NOPARITY bit was set. Note that this also means that the ECS bit is set in the status bit of every read command.

Beside the transmitted parity bit the device provides a mechanism to let the SPI master verify that the data was transmitted correct.

When the device receives a bit from the master (MOSI) then the bit is registered in the SPI input register. The **inverted** bit is send back to the master (MISO). Because the bit is registered first, the bit returned is delayed by one SCLK cycle.

Figure 6.1.11.1-1 shows the processing of an 8-bit command as an example.

After CSB has become active (CSB=0) the data provided by the master is registered at every rising edge of SCLK. The most significant bit of the command (C7) is registered with the first rising edge of SLCK and the inverted value of C7 is provided on MISO at the falling edge of SCLK. In Figure 6.1.11.1-1 this is marked with a small arrow.

When the complete command byte (C7-C0) is sent the device sends a status byte including a parity bit (PRX) and four error flags. The PRX bit is generated over all mirrored bits sent to the master and the status byte itself to provide an odd parity.

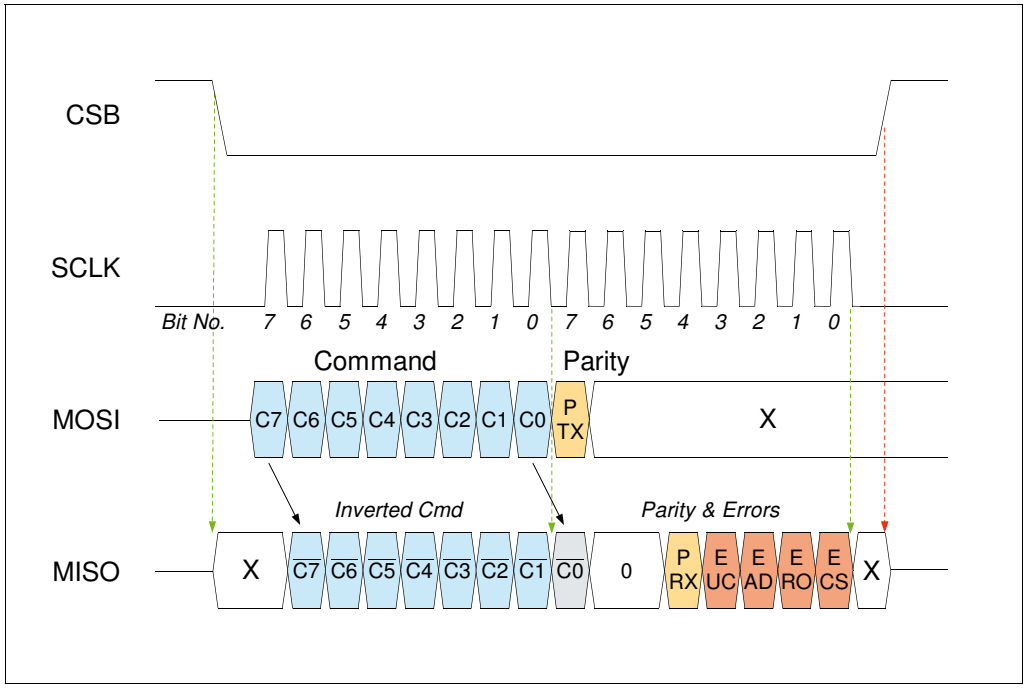


Figure 6.1.11.1-1: Bit echoing and status

Four error flags indicate problems with the command sent. If one of these bits is '1' the appropriate error has occurred. The following bits are defined:

- **EUC** (Unknown command error): The given command is not known by the device.

- **EAD** (Address error): The given address coded in the command is invalid. This might occur in read & write operations only.
- **ERO** (Read Only error): An attempt to write to a read only address was made. This might occur in write operations only.
- **ECS** (Parity error): The command or data doesn't match the (odd) parity bit.

Note that ECS is also set when a read command is processed or the NOPARITY bit in the MODE register is set. This is because in this situations no parity check is made at all and hence it can't be successful. However, in this situations the command is still executed.

A further error is signaled when the device received a valid command but is unable to execute it.

- **ENE** (Not Executable error): The command can not be executed yet.

This error is signaled by raising the **EUC** and **EAD** bits at the same time. (This normally can't happen because an unknown command
does not provide an address at all and hence that address can not be wrong.)
An ENE error occurs when a user command tries to execute a command that is not executable in the actual device state, i.e. sending a MEASURE command while
an other MEASURE command is running. An other popular example is sending a SLEEP command while the device is still running RSI or AUTOMODE measurements.
When an ENE error occurs the device does not execute the command but raises the EUC and EAD bits in the status, returned to the SPI-master.

Figure 6.1.11.1-2 shows an example of a read command. No parity bit is added to the command byte (hence no additional byte) because the whole transaction, including the command itself can be verified using the mirrored bits sent back to the master.

After the command is transferred the device starts sending the requested data (D7-D0) followed by the status byte. The position of the parity- and error bits is the same as in the write command shown above.
The two MSB's are constantly set to '0' because no data bit is unsent. (Note: On write commands the LSB of the data byte was assigned to bit 7 of the status byte.)

The ERO bit is always '0' because no write access was made at all. The ECS bit is always '1' as described above.

The only possible error situations that can occur are when an unknown command was received or an invalid address is given by the read command. This is signalled by setting the EUC bit and/or the EAD bit to '1' (marked red for reference) .

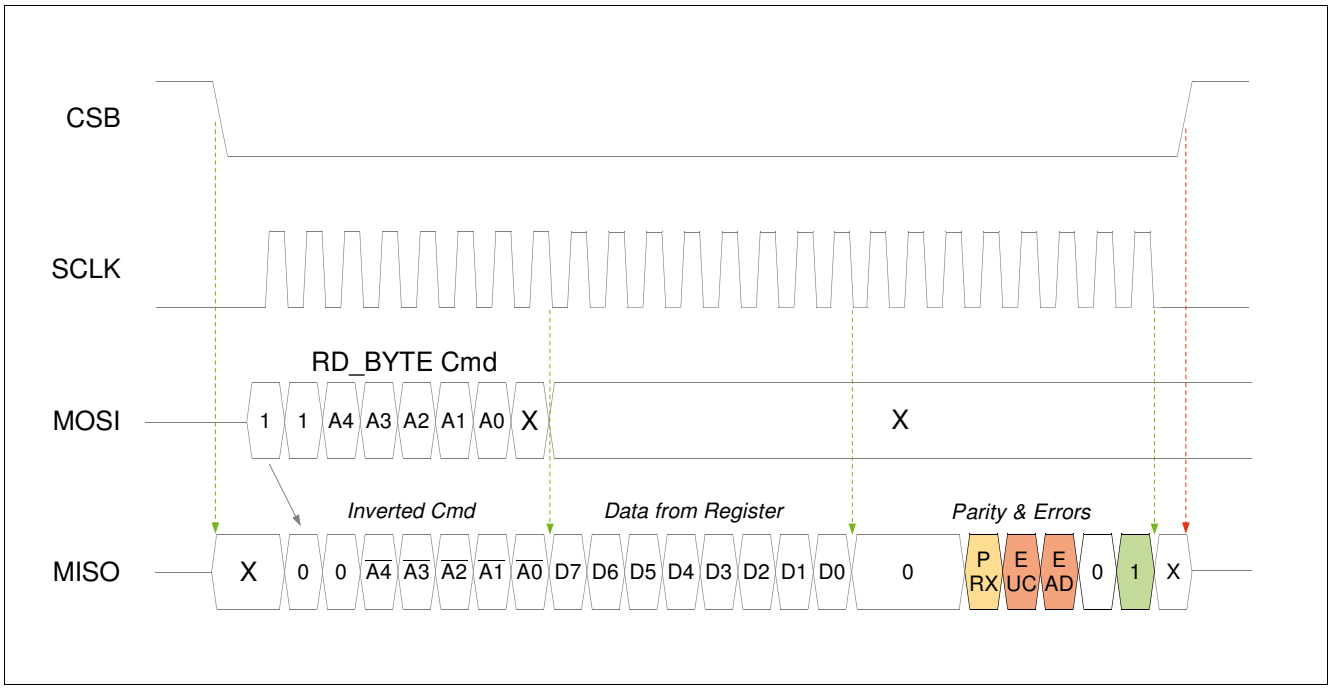


Figure 6.1.11.1-2: Read byte and CRC

The SPI features a timeout monitor to prevent communication errors due to missing SCLK edges.
During a running transaction the maximum allowed time between two SCLK edges must be less than $t_{TO(SPI)}$.

After this time the transaction is aborted and the SPI is reset to its initial state.

6.1.11.1.1 8 bit commands

8-bit commands consist of a single byte of data and an (optional) byte carrying the parity bit send from the SPI-master.
Figure 6.1.11.1.1-1 shows an example diagram for the RESET command.

After the falling edge of CSB the MISO Signal becomes active. The initial value of the MISO signal is undefined because the device has not received any data to echo yet.
The eight bits of the command are provided by the master at the MOSI signal and registered by the slave on the rising edge of SCLK.

On the falling edge of SCLK the received bits are inverted and mirrored at the MISO signal for verification as described in chapter 6.1.11.1.

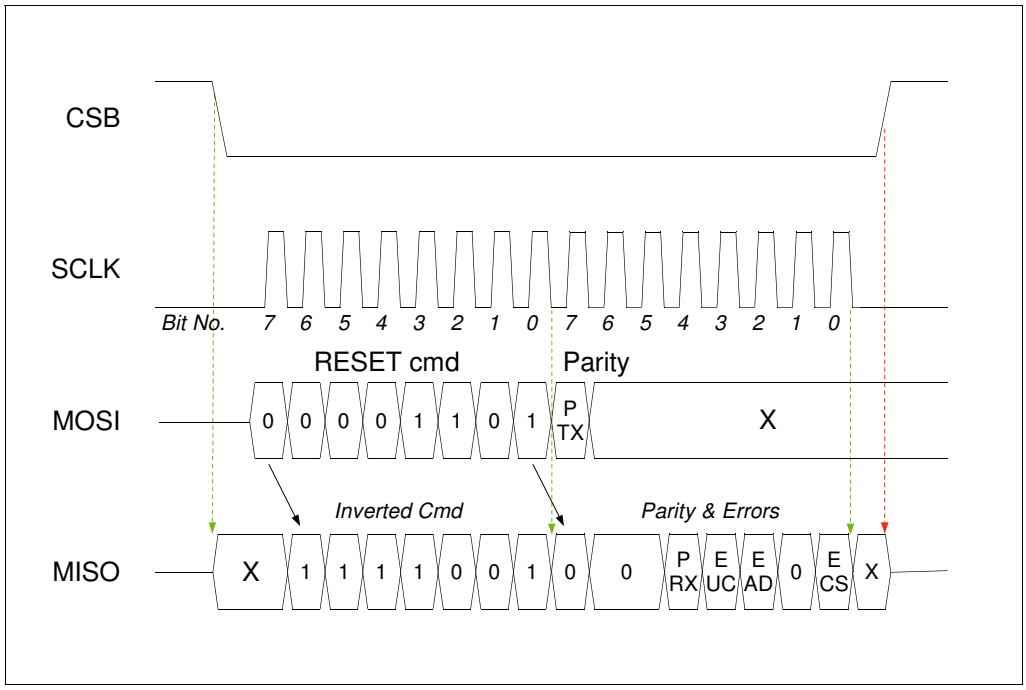


Figure 6.1.11.1.1-1: 8-Bit command

When the command byte is transferred (after eight SCLK pulses) the device provides a status byte at the MISO line for the next eight SCLK pulses while receiving the parity bit as MSB on the MOSI line. Further data on MOSI is ignored for these SCLK pulses.

When the second byte is transferred, the device verifies the command against the parity bit. When this check is successful (the parity over command byte and parity bit is odd) the command is executed.
Otherwise either the command is not known by the device or the checksum test has failed. In the first case the EUC bit is set, in the second case the ECS bit is set and the command is abandoned.

When the NOPARITY-bit is set in the MODE register the command is executed after the eight SCLK pulse unless the command is not recognised. In this case the EUC bit is set in the status byte.
An example is given in Figure 6.1.11.1.1-2.

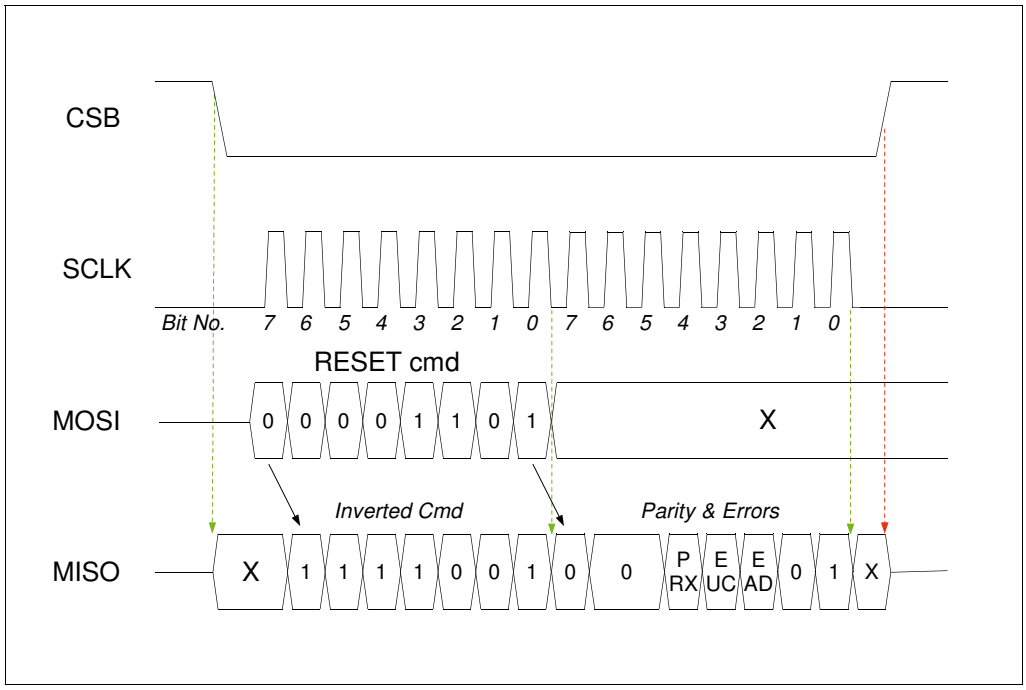


Figure 6.1.11.1.1-2: 8-Bit command without CRC

6.1.11.1.2 Write commands

The device accepts write commands for 8-bit values. A status byte, including parity- and errorbits, is returned by the device after the data transfer.

Figure 6.1.11.1.2-1 shows the transfer of a byte to a register.

After the falling edge of CSB the MISO Signal becomes active. The initial value of the MISO signal is undefined because the device has not received any data to echo yet.
On the falling edge of SCLK the received bits are inverted and mirrored at the MISO signal for verification.

The write-byte command and data are provided by the master at the MOSI signal and registered by the slave on the rising edge of SCLK.
Note that the address of the destination register is embedded into the write-byte command, shown as bits A4 .. A0.

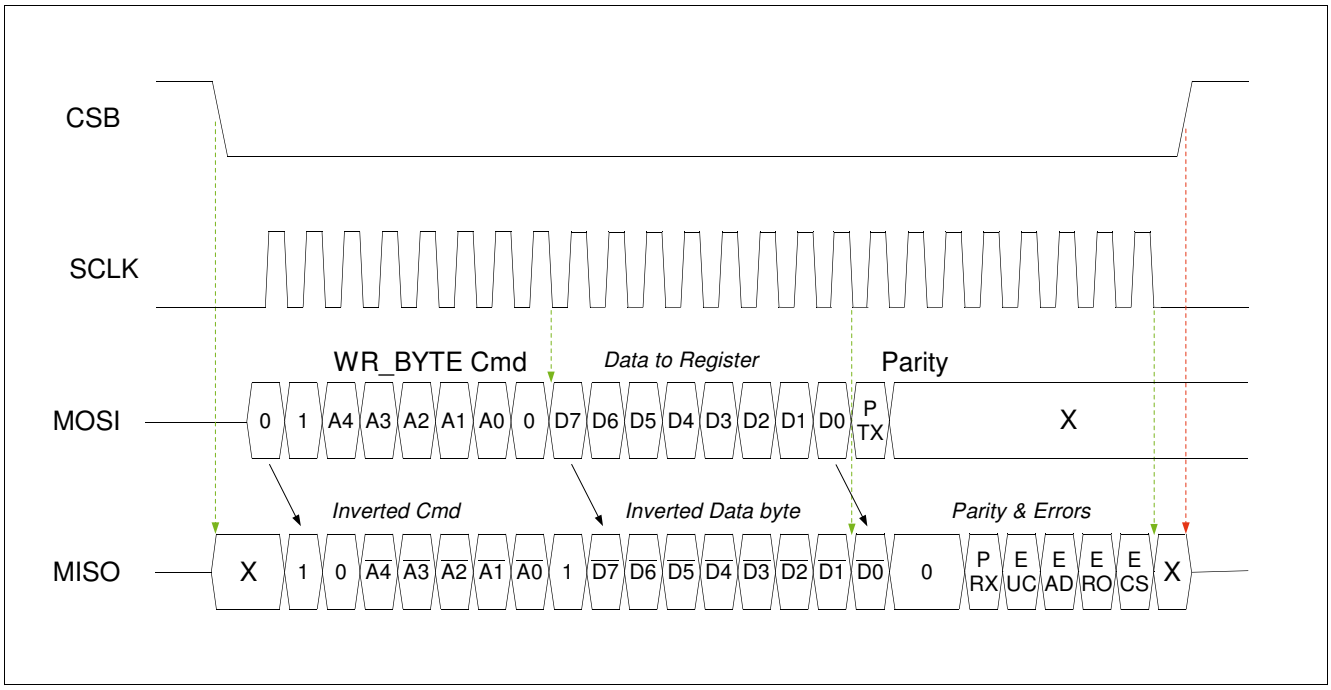


Figure 6.1.11.1.2-1: Write byte command

Finally a byte is transferred with a parity-bit as most-significant-bit.

After transmission of this byte the device verifies the transmitted command & data against the parity bit. When this verification is successful the data byte is assigned to the addressed register and a status byte is send back to the master.

Otherwise one (or more) of the following errors has occurred
- The command is not known by the device. Then the EUC-bit is set in the status byte.
- The command tries to write to an invalid address. Then the EAD-bit is set in the status byte.
- The command tries to write to a read-only register. Then the ERO-bit is set in the status byte.
- The command is correct but can't be executed yet (i.e. trying to set the RSIALS4 bit while RSI is running). Then the EUC **and** EAD bits are set to signal an ENE error.
- The checksum test has failed. Then the ECS-bit is set in the status byte.

In all of these cases the status byte is send back to the SPI master and no data is written to a register.

Finally, with the rising edge of CSB the MISO signal becomes 3-State and the SPI is set to the initial state.

Parity handling can be disabled globally by setting the NOPARITY bit in the mode register. Figure 6.1.11.1.2-2 shows the same transaction as Figure 6.1.11.1.2-1 but with NOPARITY set. Note that the ECS bit is always set as described in chapter 6.1.11.1.

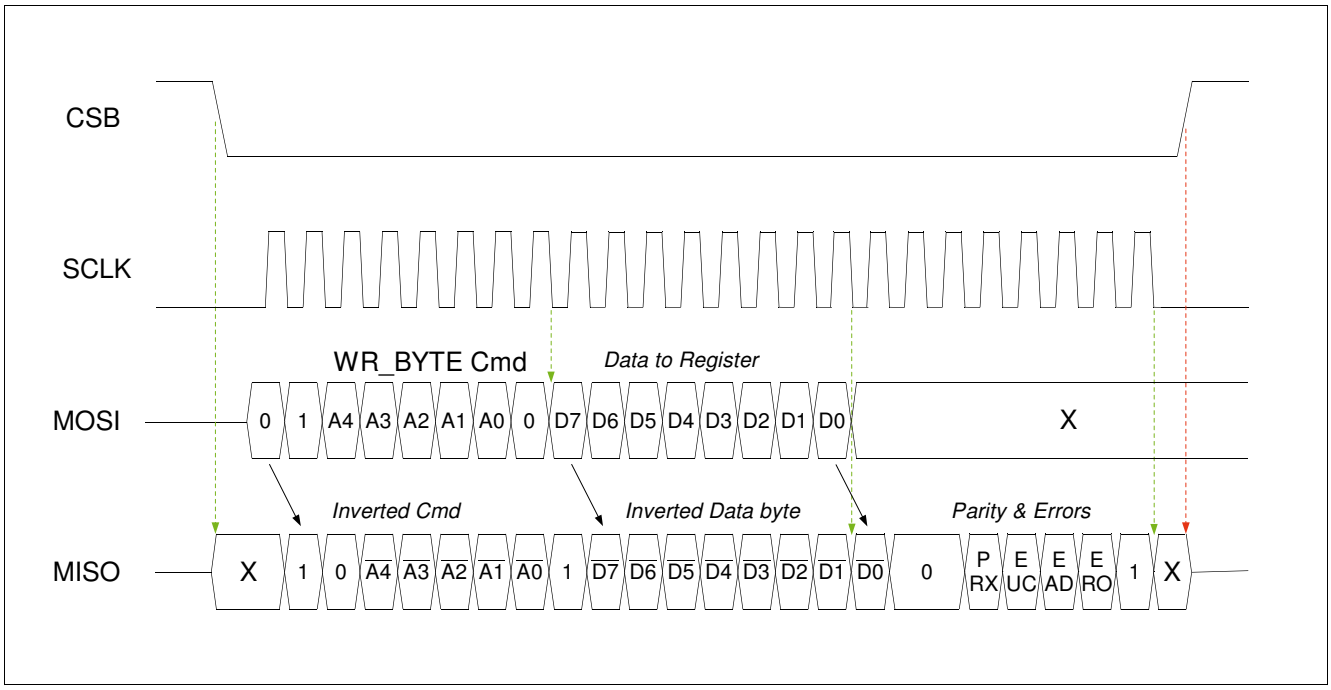


Figure 6.1.11.1.2-2: Write byte without CRC

6.1.11.1.3 Read commands

The device accepts read commands for 8-bit and 16-bit values.

Figure 6.1.11.1.3-1 shows the read operation for a single byte from a register.

After the falling edge of CSB the MISO Signal becomes active. The initial value of the MISO signal is undefined because the device has not received any data to echo yet.
On the falling edge of SCLK the received bits are inverted and mirrored at the MISO signal for verification. The last data bit is not mirrored.

The RD_BYTE command is provided by the master at the MOSI signal and registered by the slave on the rising edge of SCLK. Note that the address of the source register is embedded into the RD_BYTE command, shown as bits A4 .. A0.

When the command is transferred (after eight SCLK pulses) the device provides the content of the addressed register at the MISO line for the next eight SCLK pulses.

Finally a status byte is transferred. The status byte has the same content as described in section 6.1.11.1.2.

To keep byte-aligning of the data transmission the LSB of the command is not transferred as MSB in the second byte and hence not observable (this is in contrast to 8-bit and write commands).
To get rid of this problem the LSB of the RD_BYTE & RD_WORD commands can be either '0' or '1'. That means it doesn't care.

All data on MOSI is ignored while the device sends data or status bytes.

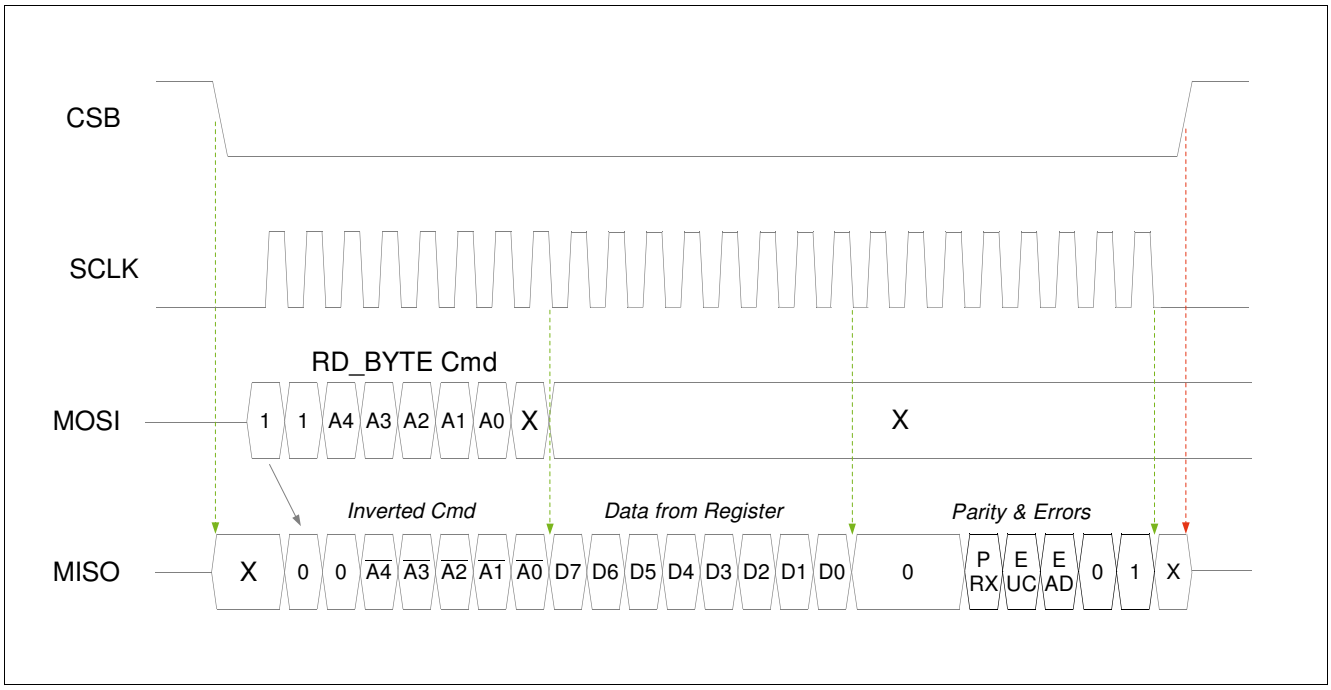


Figure 6.1.11.1.3-1: Read byte command

Note that all read command does not require sending a parity bit from the SPI master as described in chapter 6.1.11.1.

During execution the following errors can occur
- The command is not known by the device. Then the EUC-bit is set in the status byte.
- The command tries to read from an invalid address. Then the EAD-bit is set in the status byte and a zero data value (all data bits are '0') is returned.

The RD_WORD command can be used to read a 16 Bit word from two consecutive registers. An example is given in figure Figure 6.1.11.1.3-2.

RD_WORD behaves similar to RD_BYTE but generates only one status byte for the two bytes read. This is useful for reading the register pairs that contains 16- bit values spread over two consecutive registers.

Note that the address bit A0 must be set to '0' for word reads. Otherwise the device will reject the command with an EAD error.

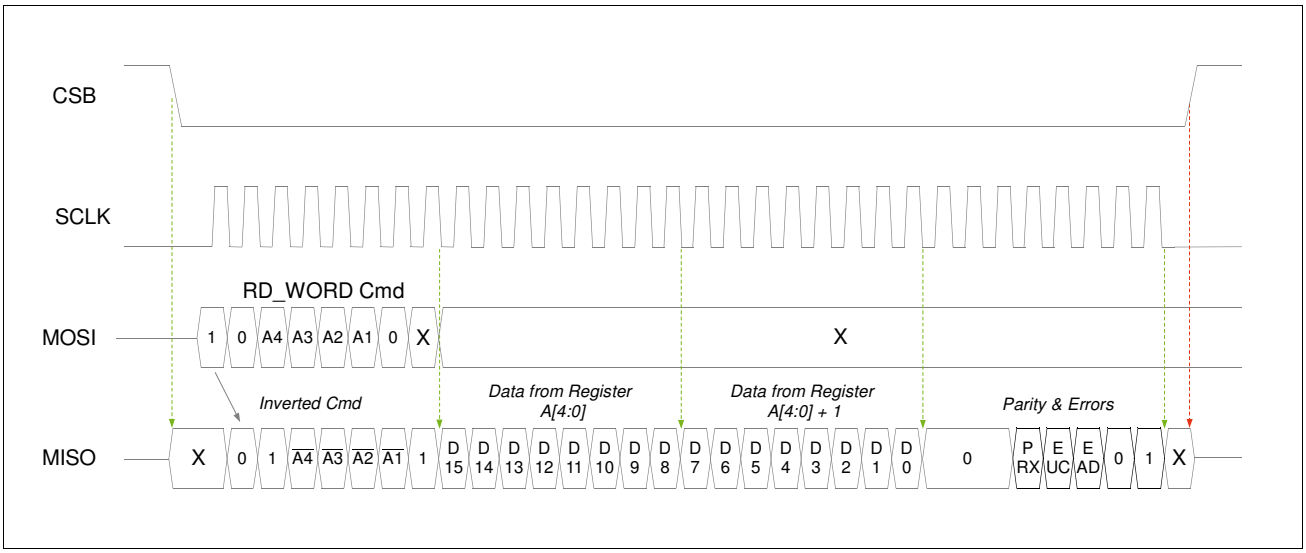


Figure 6.1.11.1.3-2: Read word

6.1.11.2 SPI Commands

The following Table Table 6.1.11.2-1 lists all SPI commands.

Table 6.1.11.2-1: SPI Command Table

Command	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	Description
NOP	0	0	0	0	0	0	0	0	No Operation
STOPMEAS	0	0	0	0	1	0	1	0	Stop repeated execution of a MEASURE command when the device is in burst measure. (Doesn't affect MEASURE commands when the device is not in burst mode)
RESET	0	0	0	0	1	1	0	1	Reset complete logic
SLEEP	0	0	1	0	0	1	0	0	Send device to sleep mode. This command is only accepted when the DEVRDY bit in the STATUS register is set and no RSI or ALS measurements are running.
MEASURE	0	0	1	1	CH_3	CH_2	CH_1	CH_0	Start a manual ADC measure. This command is only accepted the DEVRDY bit in the STATUS register is set.
WR_BYTE	0	1	A_4	A_3	A_2	A_1	A_0	0	Write a 8 bit word
RD_BYTE	1	1	A_4	A_3	A_2	A_1	A_0	X	Read a 8 bit word
RD_WORD	1	0	A_4	A_3	A_2	A_1	0	X	Read a 16 bit word

Legend :
B : b0 clear , b1 set;
A_4 to A_0 : 5 bit address;
CH_3 to CH_0 : ALS ADC measurement channel;
X unused

The commands can be divided in 8 bit commands which are executed after reading the command byte (and parity bit, if applicable), and read/write commands where the length is variable and the execution is performed during the transmission.

A special kind of command is the MEASURE command.

While other commands execute when the command (and parity, if applicable) are correct, the MEASURE command only initiates a measurement to be proce4ssed at the next possible timing slot. This ensures that running AUTOMEASURE measurements are not aborted.

The MEASUREMENT command immediately set the BUSY bit in the status register. As long as this bit is set the measurement is processing. When the requested measurement is finished the BUSY bit is cleared and the result is transferred to the ADCVAL register.

Note that the rain sensor input may be used as ALS4 input channel. Therefore a MEASUREMENT command for the RSI/ALS4 channel is skipped without further notice (i.e. no error is raised) when the rain sensor interface is running (RUNRSI bit is set).

The channels that can be measured with the MEASUREMENT command are given in table Table 6.1.11.2-2 below.

Table 6.1.11.2-2: Channel assignment for the MEASUREMENT command

Channel number	***Channel name***	***column3***
0	ALS0	Input current of ambient light sensor 0
1	ALS1	Input current of ambient light sensor 1
2	ALS2	Input current of ambient light sensor 2
3	ALS3	Input current of ambient light sensor 3
4	RSI/ALS4	Input current of rain sensor (measured via ALI-ADC)
5	ICAL	Internal ALI calibration current, Note: To measure the ALI calibration current additional settings (calibration register) must be made.
6	VTEMP	Internal temperature sensor
7	VREF	Reference voltage at pin VREF (only for diagnose)
8	RSIINT	Output of the RSI integrator (only for diagnose)
9	VIREF	Voltage of ALI-IREF current over an internal resistor (only for diagnose)
10	VDDD	Internal divided digital supply voltage (only for diagnose)
11	VDDA	Internal divided analog supply voltage (only for diagnose)
12	VBG	Internal bandgap voltage (only for diagnose)
13	reserved	Reserved, do not use
14	reserved	Reserved, do not use
15	reserved	Reserved, do not use

6.2 LIN Module

6.2.1 Overview

The LIN SBC module is the interface between the physical bus in a Local Interconnect Network (LIN) and the LIN master / slave protocol controller after LIN 2.1 specification. Due to slew rate control of the LIN output it provides optimum EMC performance.

6.2.2 LIN Module Operating Modes

The LIN SBC module provides the following operation modes:

- **Power-off mode**: The battery voltage was falling under the power down threshold level. The voltage regulator is switched off. The device will be given a power on reset (pin **RES_N** activated) in case the battery voltage level exceeds the $V_{VS,POR}$ threshold level.
- **Power-on mode**: The device is powered by a battery voltage above POR reset level and is waiting for activation by pin **EN** from the microcontroller. The voltage regulator is switched on. The watchdog is active.
- **active mode**: The physical LIN transceiver is activated. The voltage regulator and the watchdog are active.
- **Standby mode**: The LIN transceiver is switched off. The voltage regulator is active. The watchdog is inactive. The wake up sources are enabled. The device consumes low current.
- **Sleep mode**: The LIN transceiver is off, the voltage regulator is shut down and the watchdog is inactive. The wake up sources are enabled. The device consumes very low current.
- **Flash mode**: The slew rate control and the receiver filter are switched off in order to achieve a high data baud rate for microcontroller flashing. The voltage regulator and the watchdog are active.

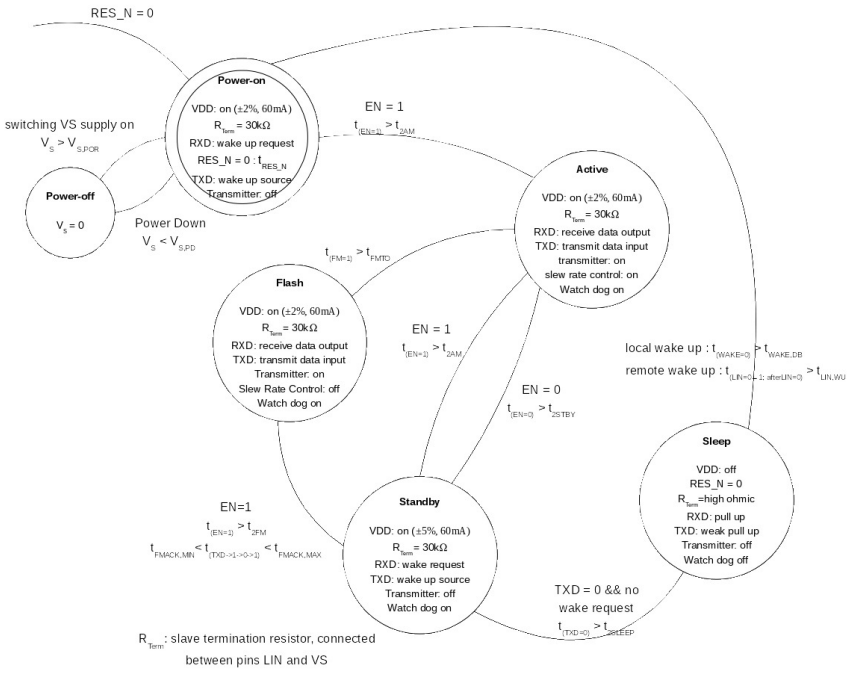


Figure 6.2.2-1: SBC State Diagram

Table 6.2.2-1: Pin Functionality

Mode	*EN*	*VDD*	*RXD*	*TXD*	*LIN*	*Watch Dog*
Power-off	high impedance	off	high impedance	high impedance	high impedance	off
Power-on	low	on	strong pull down output for wake up request	weak pull up output if remote wake up; strong pull down output if local wake up	off	on after RES_N is high
Active	high	on	pull up for LIN recessive; strong pull down output for LIN dominant	high level input for LIN recessive; low level input for LIN dominant	on; slew rate control activated	on
Standby	low	on	strong pull down output for wake up request	weak pull up output if remote wake up; strong pull down output if local wake up	transmitter off termination on	on
Sleep	low	off	pull up	pull down	off	off
Flash	high	on	pull up for LIN recessive; strong pull down output for LIN dominant	high level input for LIN recessive; low level input for LIN dominant	on; slew rate control deactivated	on

6.2.2.1 Power-off Mode

The device enters Power-off mode in case the battery voltage is lower than $V_{S,PD}$ voltage level. In Power-off mode the voltage regulator is switched off. If the battery voltage rises above the power on reset threshold level $V_{S,POR}$ the device resets the system via activating pin **RES_N**. The device enters mode Power-On.

6.2.2.2 Power-on Mode

When the voltage at pin **VS** exceeds the Power-on-reset threshold voltage $V_{S,POR}$, the device enters Power-on mode. In that mode the voltage regulator is switched on. After pin **VDD** exceeds $V_{DD,RSTD}$, RES_N is held low for t_{RES_N}. Now with setting pin **EN** to active HIGH level for a time period of at least t_{2AM} the device enters Active mode. Any wake up request from mode SLEEP is indicated to the interrupt input of the microcontroller by setting the pin **RXD** to LOW level.
The wake up source can be recognized by the microcontroller by reading the level at pin **TXD**. A weak pull up indicates a remote wake up request and strong pull down indicates a local wake up request.
Note: The voltage regulator over temperature shut down results in a transition to Power-on mode and the regulator is switched off. The voltage regulator will be switched on, only if the junction temperature falls below the specified temperature hysteresis T_{HYST}.

6.2.2.3 Active Mode

In Active mode the device is able to transmit and receive data via the LIN bus line. The receiver transfers the detected LIN bus data via pin **RXD** to the microcontroller: HIGH at a recessive level and LOW at a dominant level on the bus. The receiver has a **VS** supply related threshold with hysteresis and an integrated filter to suppress bus line EMI. The transmit data at the **TXD** input is converted by the transmitter into a LIN bus signal. The LIN bus slew rate is optimized to minimize EME. The LIN bus output pin is pulled HIGH via an internal slave termination resistor. For a master application an external resistor in series with a diode should be connected between pin **VS** on one side and pin **LIN** on the other side.
The device enters Active mode from Standby mode or Power-up mode whenever a HIGH level on pin **EN** is maintained for a time of at least t_{2AM}. The device enters Active mode from Flash mode after a time out of t_{FMTO}.
The device enters Standby mode from Active mode in case of a LOW-level on pin **EN**, maintained for a time of at least t_{2STBY}.

6.2.2.4 Standby Mode

In Standby mode the voltage regulator is activated. Also the slave termination resistor at pin **LIN** is enabled. The watch dog is running.
Any wake up request is indicated to the interrupt input of the microcontroller by setting the pin **RXD** to LOW level. The wake up source can be recognized by the microcontroller by reading the level at pin **TXD**. A weak pull up indicates a remote wake up request and strong pull down indicates a local wake up request.

6.2.2.5 Sleep Mode

The Sleep mode is a very low power mode of the device. The supply current in Sleep mode is typically 5 µA.
After entering Standby mode a **TXD** LOW level for at least t_{2SLEEP} will result in entering Sleep mode. The transition to sleep mode can be performed independently from the actual level on pin **LIN** or pin **WAKE_N**. In Sleep mode the voltage regulator is deactivated and becomes high ohmic after a delayed time of $t_{DD,OFFDEL}$.
The transition into mode Sleep is prohibited if a wake up request is pending. The request must be cleared via a transition to mode Active.
In Sleep mode the internal slave resistor termination at LIN bus pin is switched off. A power-saving weak pull-up between pins **LIN** and **VS** is still present.
The device can be woken up remotely via pin LIN or locally via pin **WAKE_N**. Debounce filters prevent unwanted wake-up events due to EMI at the inputs of the wake-up sources.

6.2.2.6 Flash Mode

Flash mode is initiated by a rising edge on pin **EN** in Standby mode and a command at pin **TXD** to prevent transition to Active mode. Flash mode is like Active mode with the exception of disabled LIN bus slew rate control. This is to support high baud rate microcontroller flashing via LIN bus. To enter Flash mode the pin **EN** must be set HIGH for at least t_{2FM} and after this the pin **TXD** must be acknowledge Flash mode access with an LOW pulse t_{FMACK} in time period t_{2AM} . The Flash mode is left to Active mode after time out t_{FMTO} .

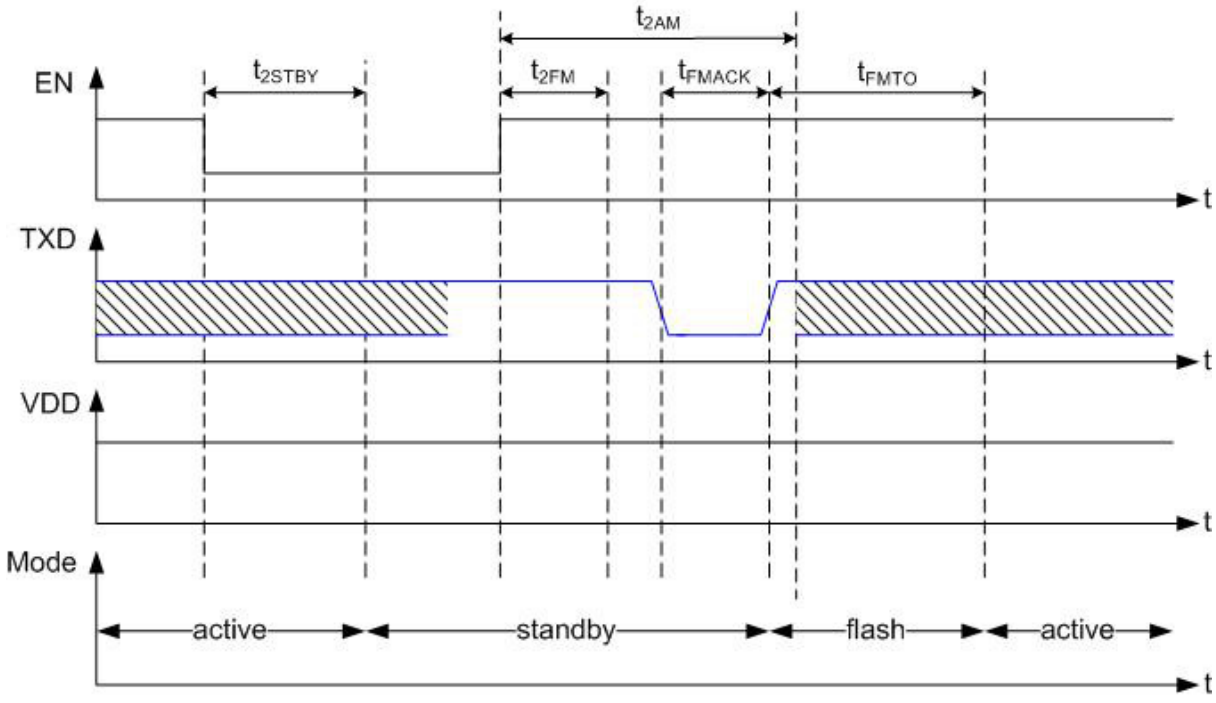


Figure 6.2.2.6-1: Flash mode transition timing with TXD acknowledge pulse.

6.2.3 Fail Safe System

6.2.3.1 Reset Parameters

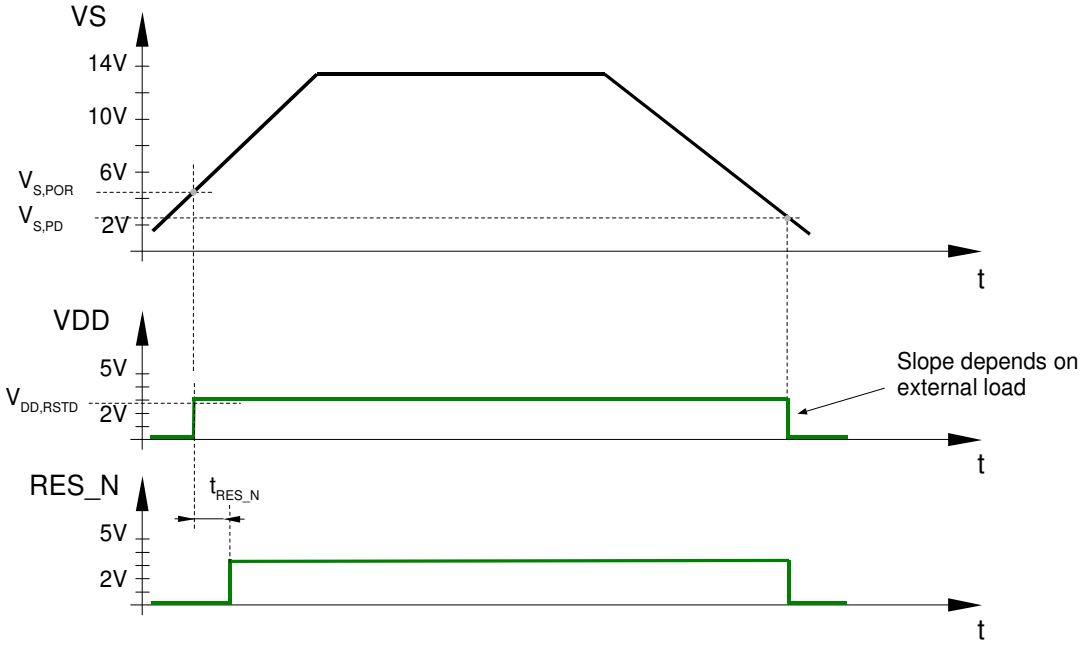


Figure 6.2.3.1-1: Power up and power down behaviour at VDD and RES_N regarding to VS in 3.3 V mode

The regulator is switched off when the voltage at pin **VS** falls under $V_{S,PD}$ threshold. The slope of the falling edge at pin **VDD** depends on the external load.

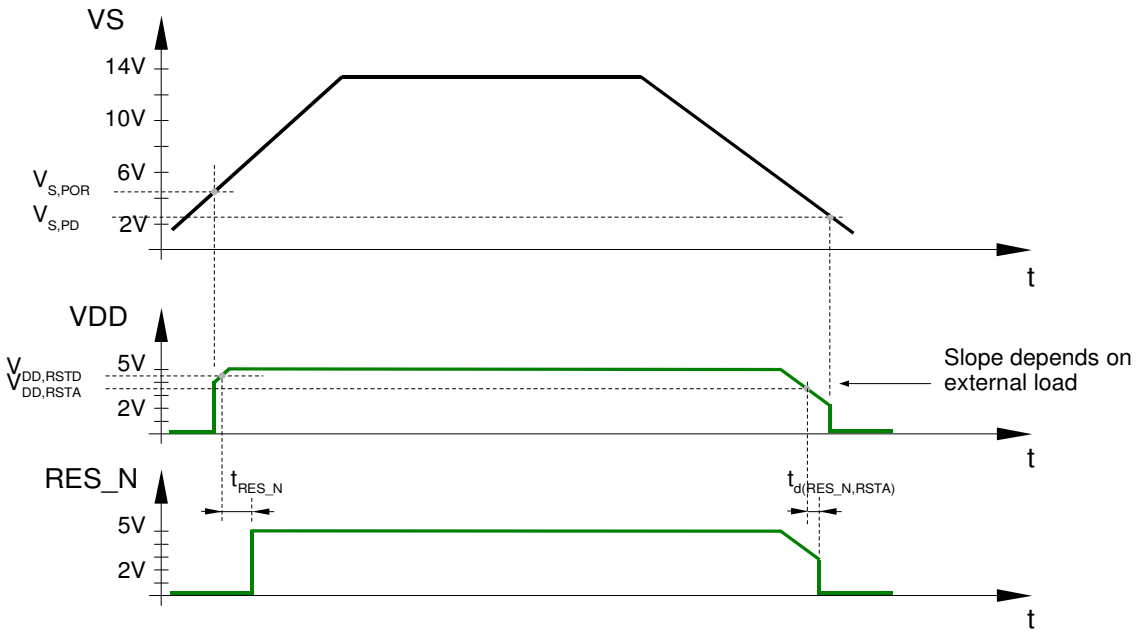


Figure 6.2.3.1-2: Power up and down behaviour at VDD and RES_N regarding to VS in 5 V mode

The regulator is switched off when the voltage at pin **VS** falls under $V_{S,PD}$ threshold. The slope of the falling edge at pin **VDD** depends on the external load.

6.2.3.2 Pin Termination

There are pin termination for fail-safe operating conditions:

Table 6.2.3.2-1: Fail-Save Pin-Termination Table.

Pin	*Termination*	*Reason*
WDDM	weak pull down	set WD active in case of floating pin **WDDM**
TXD	weak pull up	set TXD input to defined level in case of floating pin **TXD**
EN	weak pull down	force SBC in Sleep mode in case of floating pin **EN**
WDIN	weak pull down	terminates WD trigger input in case of floating pin **WDIN**; results in activating **RES_N**

6.2.3.3 Thermal shutdown

The LIN-SBC is protected against thermal stress. In case the junction temperature exceeds the shutdown junction temperature T_{SHDN}, the internal SBC thermal shutdown flag is set. The flag is reset in case the junction temperature is lowered about T_{HYST} independently.

The SBC behaves different whether the over temperature flag is caused by the voltage regulator power dissipation or the LIN transmitter power dissipation. In any
case it shut down the detected heat source and limits power dissipation of the SBC.

6.2.3.4 LIN over current protection

The output current of the LIN transmitter is limited to $I_{LIN,LIM}$ in order to protect the transmitter against short circuit to pin **VS** .

In order to limit power dissipation caused by the LIN transmitter the LIN BUS is monitored in the dominant state, i.e. **TXD=0**: If the LIN bus voltage level exceeds $V_{LIN,OV}$ for debouncing time $t_{LIN,OV}$ and the SBC thermal shutdown flag is set the LIN transceiver will be set high ohmic. The LIN over temperature flag is set.

The LIN transmitter transmit TXD again in case the junction temperature is lowered about T_{HYST}, i.e. the SBC thermal shut down flag is reset. This also resets the LIN over temperature flag.

Note: The LIN shut down does not result in any state change.

6.2.3.5 Voltage regulator over current protection

In case of shorts at pin **VDD** the output current of the voltage regulator is limited to $I_{DD,LIM}$. In order to limit power dissipation of the device the voltage regulator is shut down in case the SBC thermal shutdown is set and the LIN overvoltage flag is not set. A debounce filter of $t_{DD,SHDN}$ is applied to regulator shut down.

The voltage regulator is switched on again in case the junction temperature is lowered about T_{HYST} (i.e. SBC thermal shutdown flag is reset) independently of pin **EN**.

Note: The VDD shut down does result in mode change, if the pin **VDD** voltage drops below the reset assert threshold level $V_{DD,RSTAXX}$. In this case the device enters Power-on mode.

6.2.3.6 LIN ground loss

In case of battery voltage loss (pin **VS**) and ground loss (pin **GND**) there are no reverse currents from the LIN bus line.

6.2.3.7 Power On Reset

The battery voltage is monitored during power up. If the battery voltage is above $V_{S,POR}$ level the voltage regulator will be switched on and the device enters Power-on mode.

6.2.3.8 System Reset

In case the voltage at pin **VDD** drops below the reset threshold $V_{DD,RSTAXX}$ the SBC reset pin **RES_N** is activated and pulled down to GND. This is to reset the host MCU because the peripheral voltage may be unsafely low. The reset pin **RES_N** is released after the VDD voltage exceeds the reset de-assert level $V_{DD,RSTDXX}$.

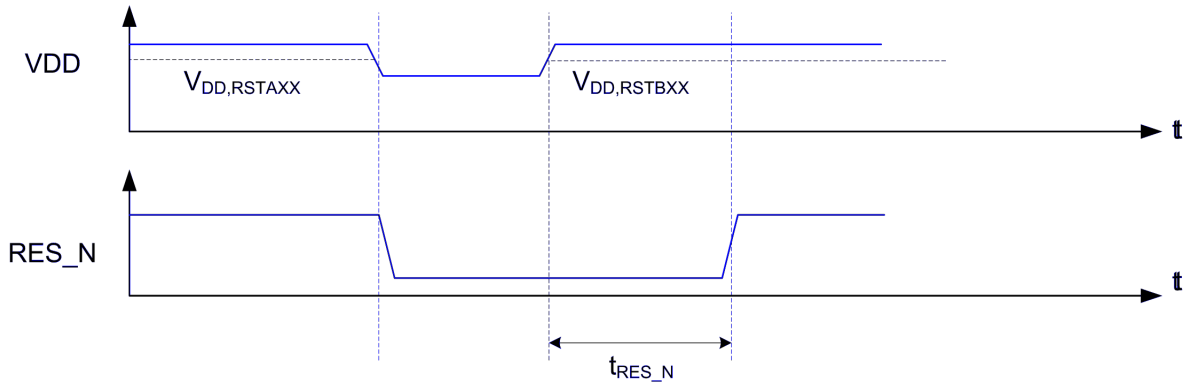


Figure 6.2.3.8-1: RES_N via VDD UV

Behaviour of pin 'RES_N' in case of 'VDD' undervoltage

6.2.3.9 Safe Power Down

In case the battery voltage drops below $V_{S,PD}$ level, operating the LIN-SBC may not be save any more. In this case the device will enter Power-off mode safely. The device powers up again if the battery voltage exceeds $V_{S,POR}$ level again.

6.2.4 Wake Up

In case the device is in Sleep mode there are 2 events to wake up the device:

1. Local wake-up with low level at pin **WAKE_N**.
2. Remote wake-up via a dominant bus state of at least $t_{LIN,WU}$.

Any of these wake up events changes the device mode from Sleep mode to Power-on mode.

6.2.4.1 Local Wake Up; pin WAKE_N

The device can be woke up from Sleep mode via pin **WAKE_N**. Pulling pin **WAKE_N** below $V_{WAKE\_N,INL}$ level results in a local wake up request.

The wake up event is falling edge triggered. This allows the device to enter
Sleep mode with pin **WAKE_N** pulled to low.

The pin **WAKE_N** is an high voltage input with pull up current source $I_{WAKE\_N,PU}$ and an input debouncer with filter time $t_{WAKE\_N,DB}$.

If the local wake up is not used in application, the pin **WAKE_N** has to be connected to pin **VS**.

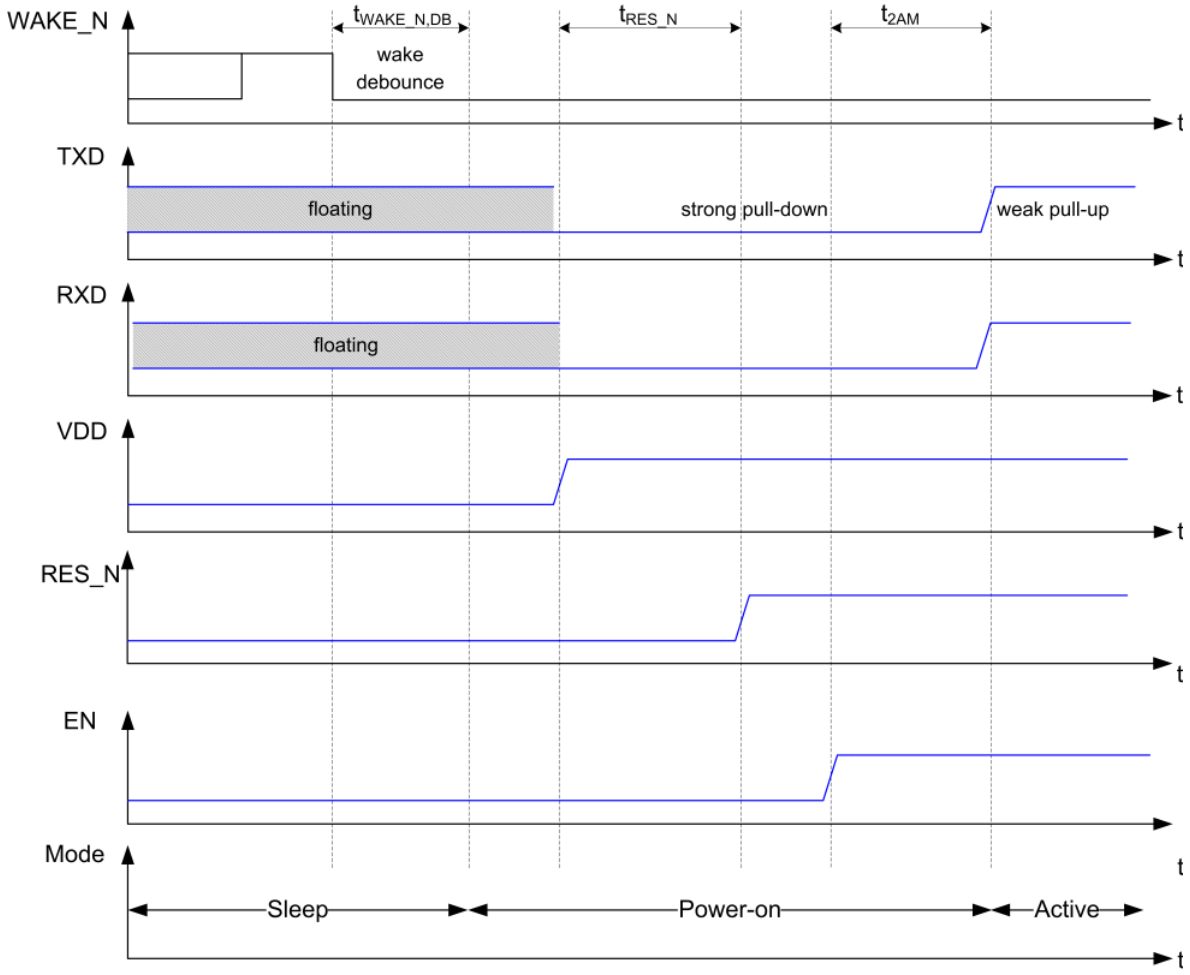


Figure 6.2.4.1-1: local wake up in mode Sleep

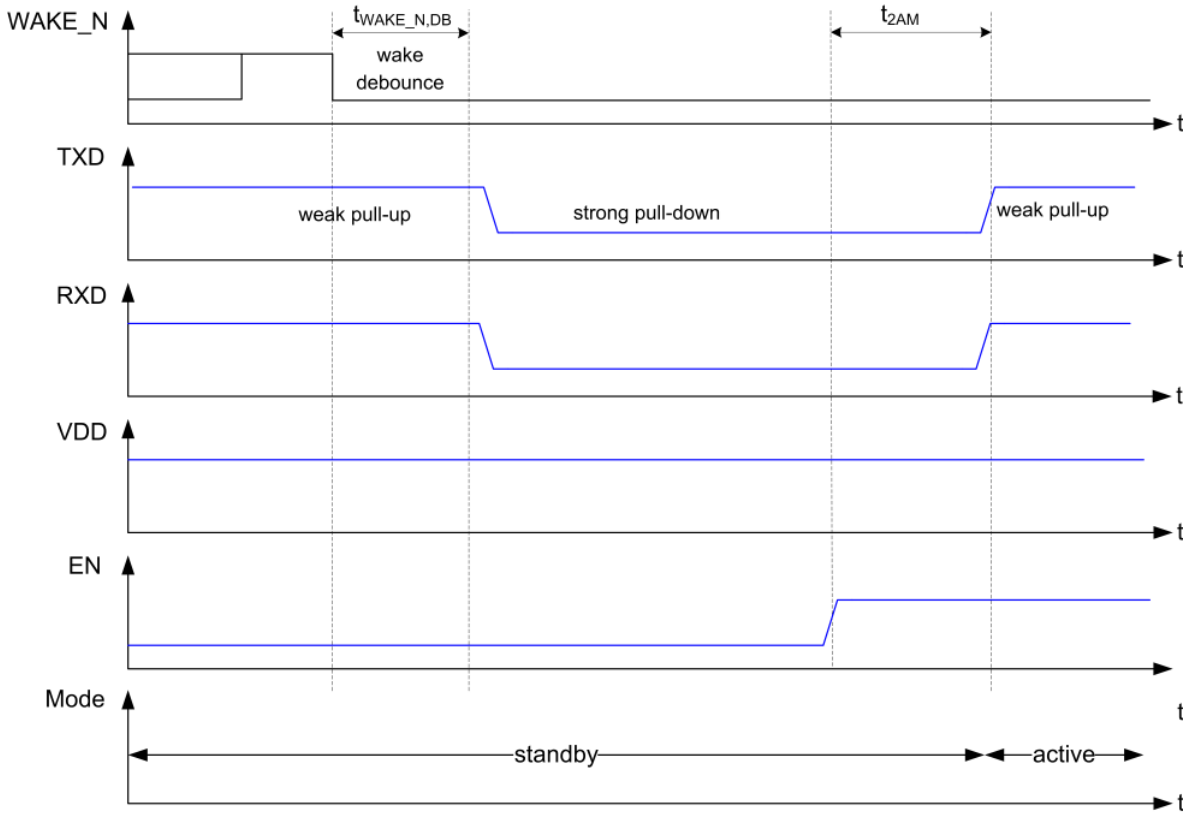


Figure 6.2.4.1-2: local wake up in mode Standby

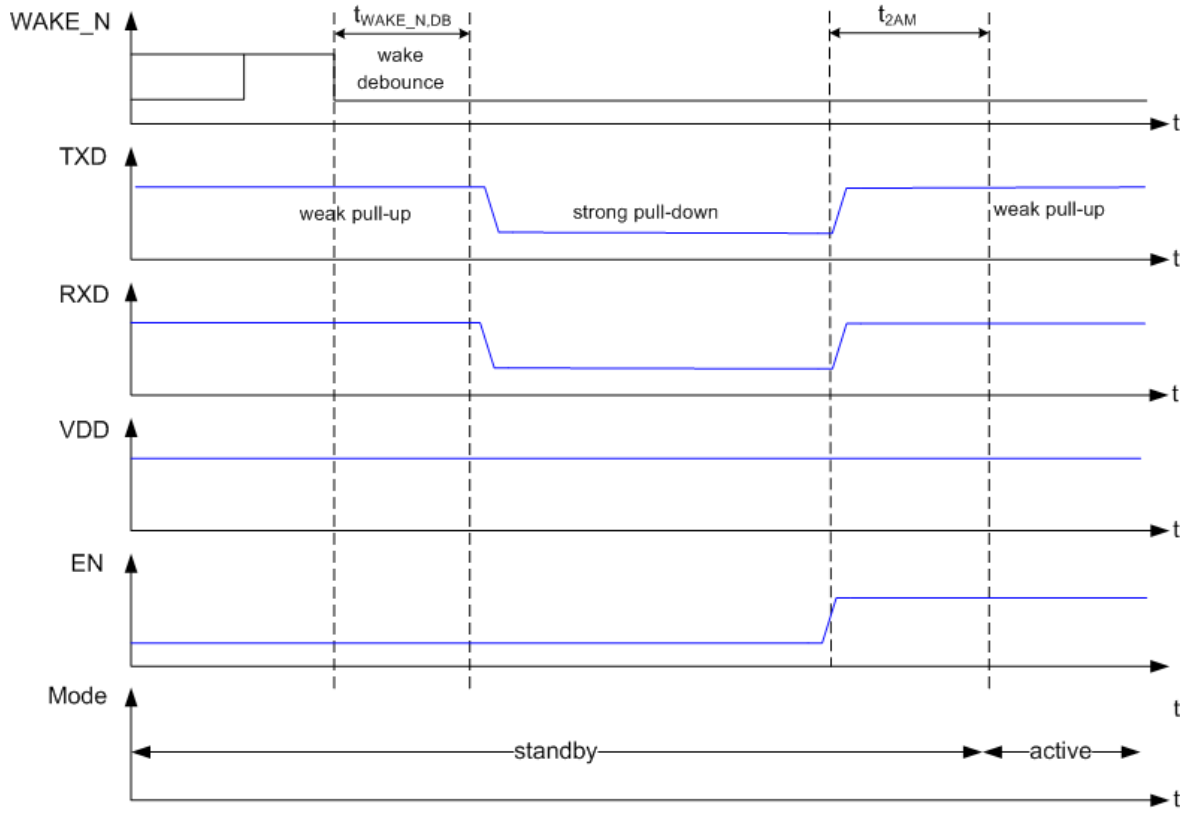


Figure 6.2.4.1-3: local wake up in mode Standby with flash mode option

6.2.4.2 Remote Wake Up

The device can be woke up remotely from Sleep mode via pin **LIN**.

A falling edge at the **LIN** pin followed by a dominant bus level $V_{LIN,DOM}$ maintained for a time period $t_{LIN,WU}$ result in a remote wake up request.

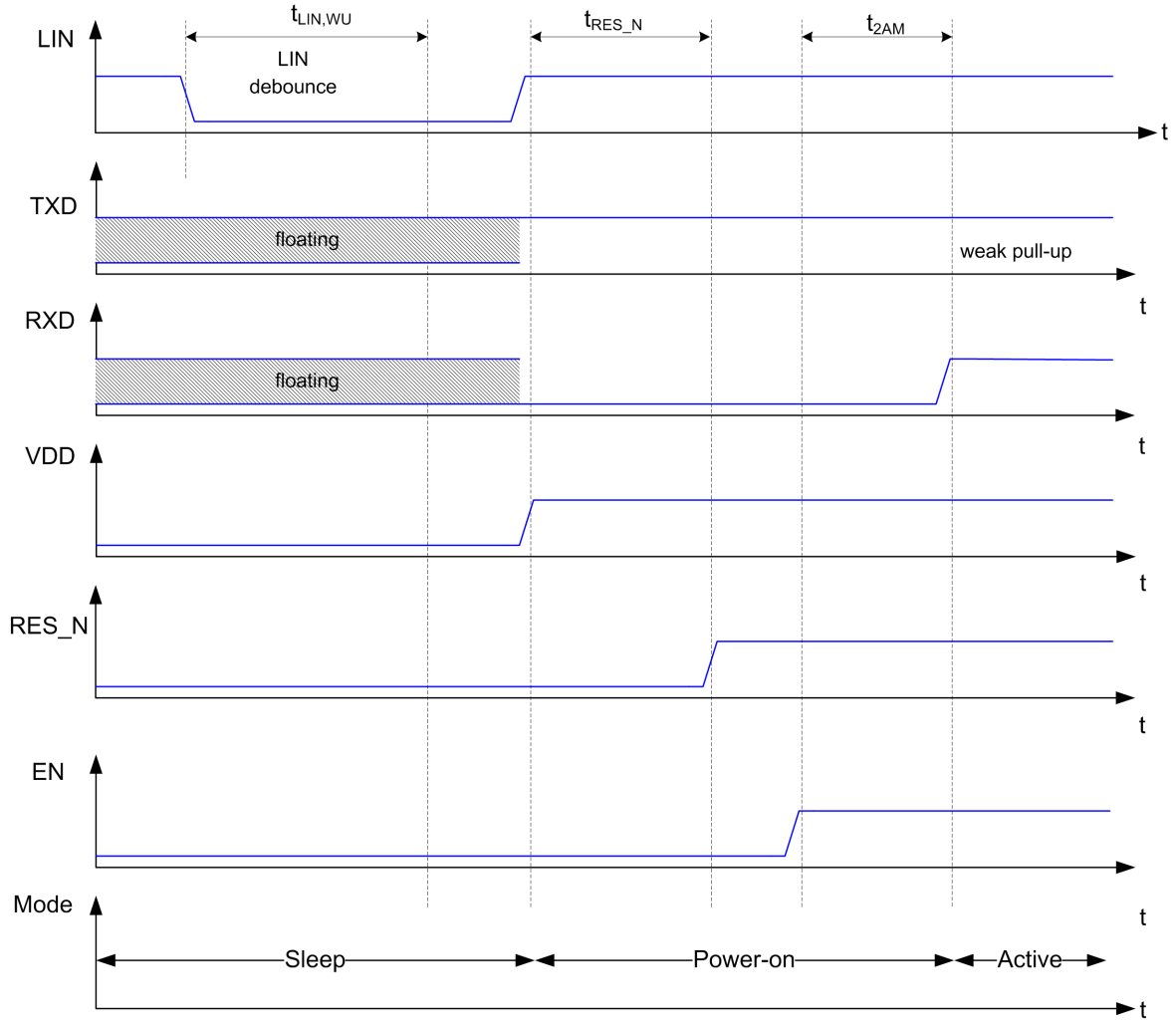


Figure 6.2.4.2-1: remote wake up in mode Sleep

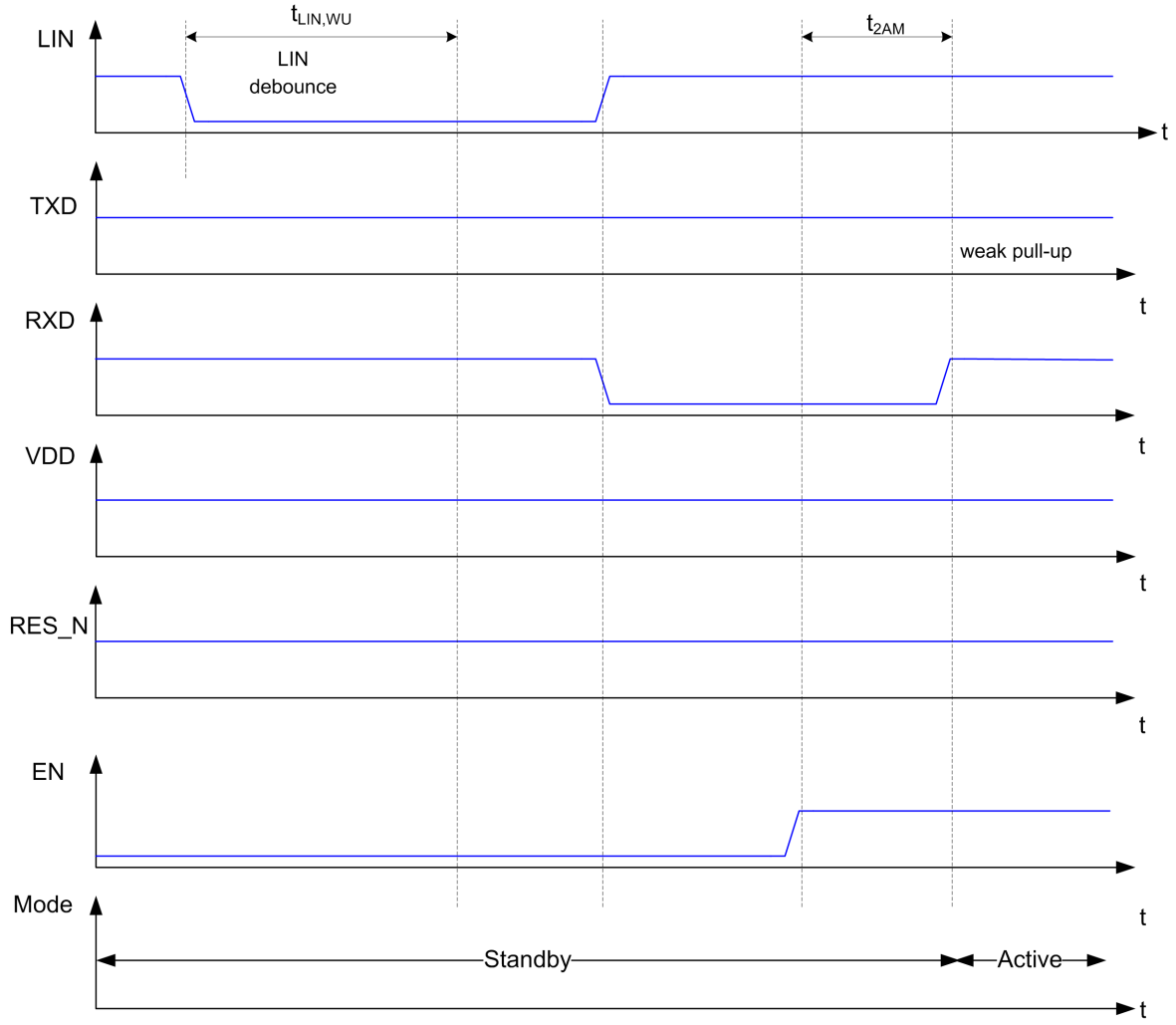


Figure 6.2.4.2-2: remote wake up in mode Standby

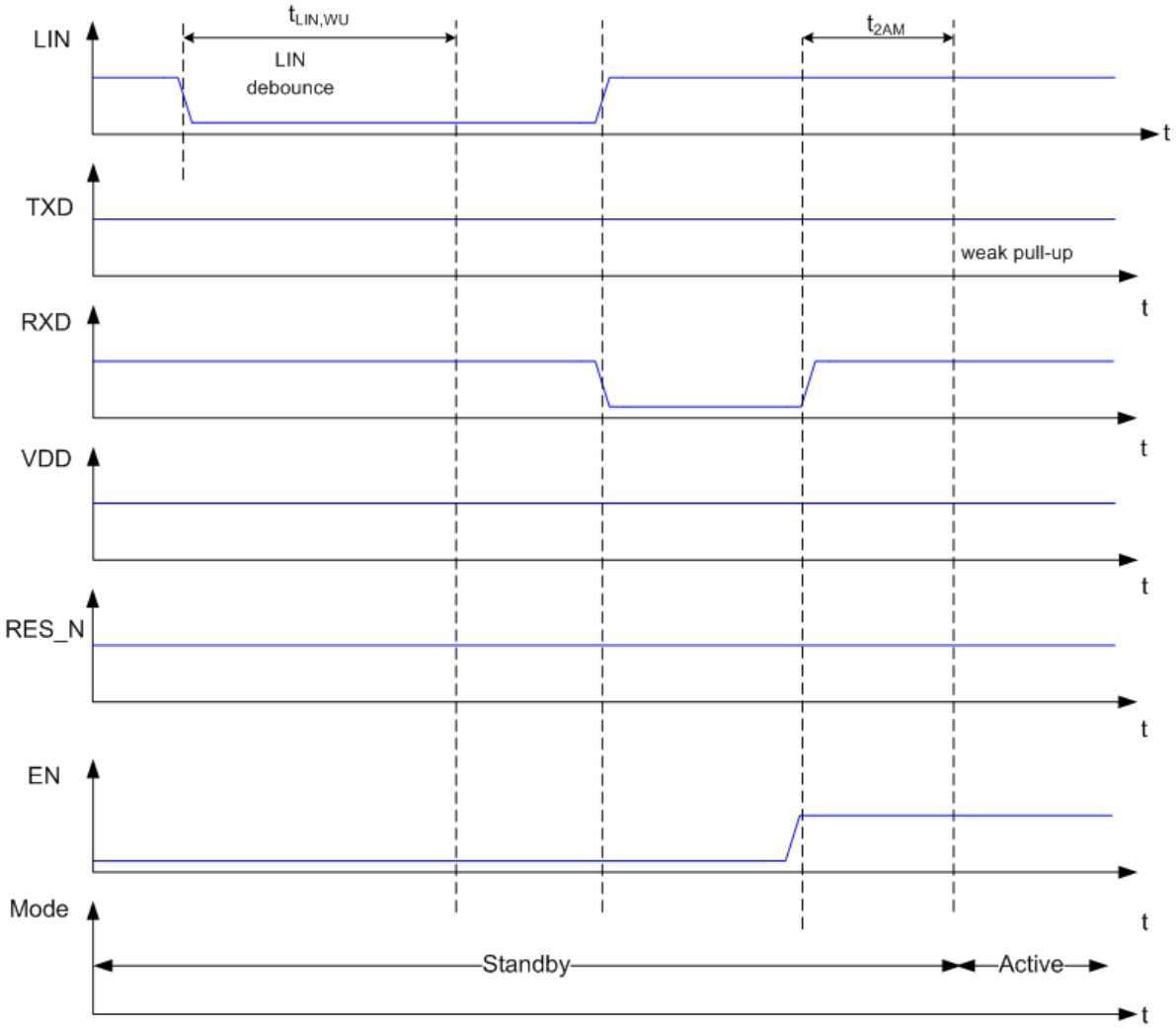


Figure 6.2.4.2-3: remote wake up in mode Standby with flash mode option

6.2.4.3 Remote and Local Wake Up Transition

In case of mode Sleep and a remote or local wake up occurs the device enters mode Power-on. In case of mode Standby and a remote or local wake up occurs the device remains in mode Standby. A transition to mode Sleep is prohibited.

6.2.4.4 Local and Remote Wake Up Source Recognition

The device latches the information of the wake up source to distinguish between a remote wake up request via dominant LIN bus and local wake up via pin **WAKE_N**. The wake up source can be read on pin **TXD** in the mode Standby and Power-on.
A HIGH level at pin **TXD** indicates a remote wake-up request (weak pull-up at pin **TXD**) and a LOW level indicates a local wake-up request (strong pull-down at pin **TXD**).

6.2.4.5 Wake-Up Flag Reset

The wake up request flag and the wake up source flag are reset after entering mode Active. The signaling at TxD and RxD are interrupted when pin **EN** is set to high in order to check flash mode request at TxD.

6.2.5 Voltage Regulator; pin VDD

The on chip low drop voltage regulator provides the voltage V_{DD} (typ. 3.3V) at pin **VDD**. It supplies the peripheral circuitry of the SBC and the host MCU chip with typical 60mA.

The voltage regulator is activated in all operating modes except in Sleep mode. In Sleep mode the voltage regulator is switched off.

The voltage regulator is limited in output current of typical 100mA. The current limitation is always activated.

6.2.6 Watchdog

The watchdog is realized as window watchdog. The watchdog is used to check whether the MCU is still running properly. It runs on watchdog oscillator clock with time base $t_{WD,OSCXX}$. The MCU will continuously retrigger the watchdog in the open window time $t_{WD,OW}$ by a specific trigger command at pin **WDIN** and no watchdog error will appear. A correct WD-trigger command in an open window starts the next closed window. Any WD-trigger command in the closed window resets the watchdog and will assert pin **RES_N**. There is a first trigger latency implemented: After **RES_N** goes high an enlarged open window starts. The first trigger command is allowed to appear latest at $t_{WD,FOW}$.
The watchdog is disabled in state Sleep. The watchdog starts with first open window after re-entering mode Active or Power-on.

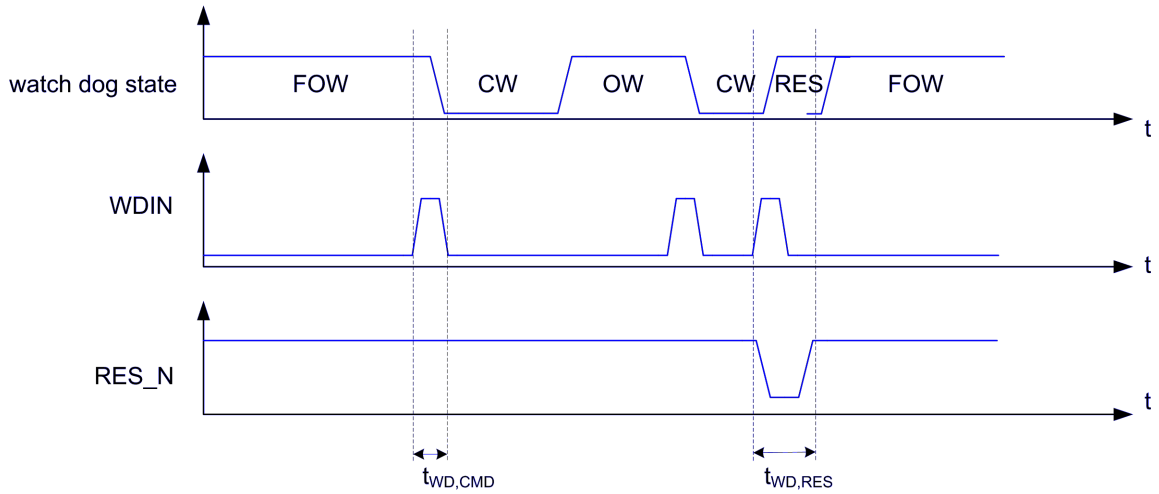


Figure 6.2.6-1: WD Trigger in CW

Behaviour of watch dog in case of trigger in closed window.

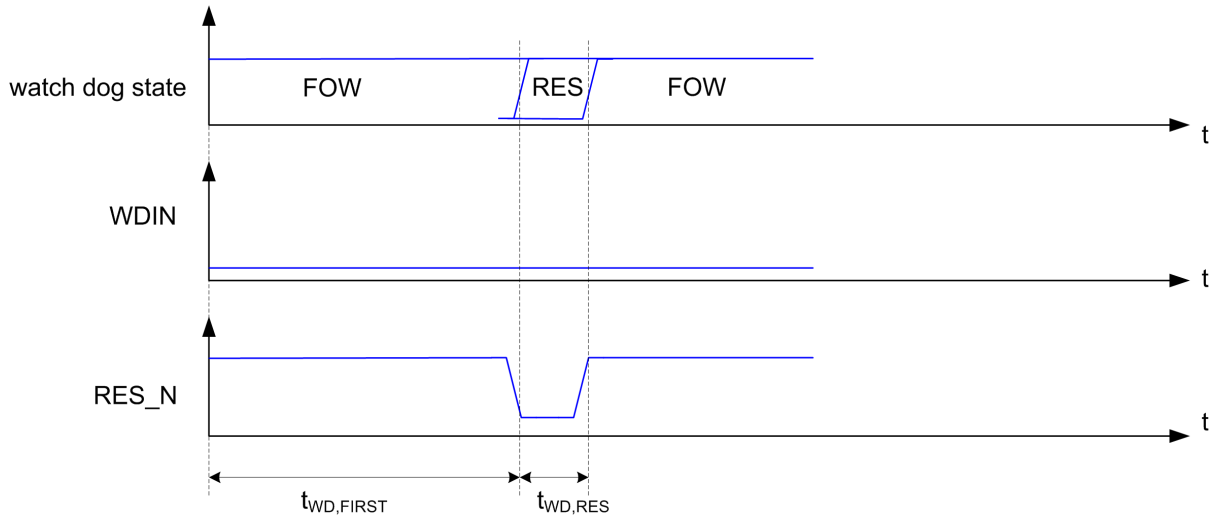


Figure 6.2.6-2: WD No Trigger In FOW

Behaviour of watch dog in case of missing trigger in open window.

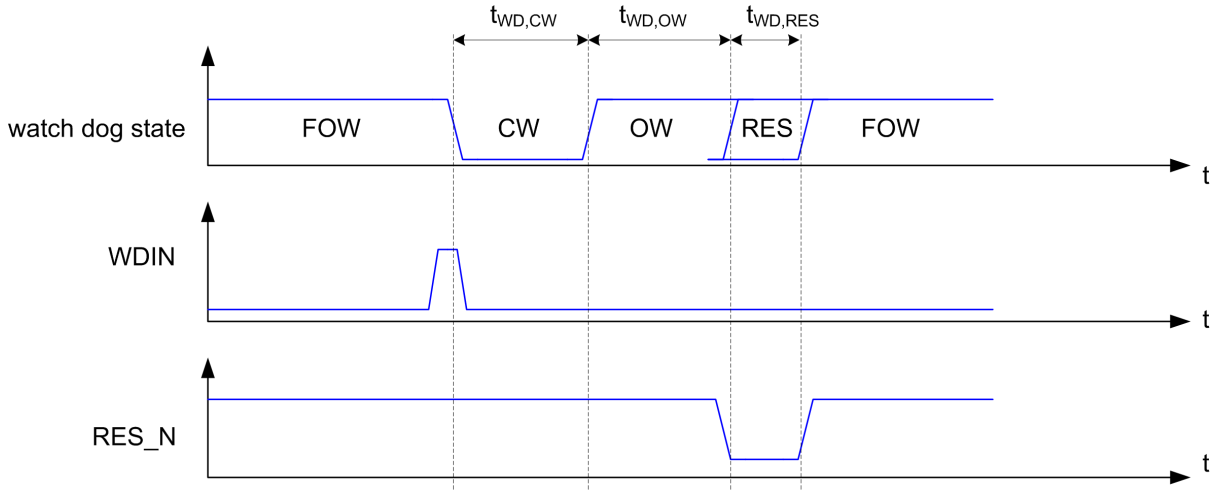


Figure 6.2.6-3: WD No Trigger In OW

Behaviour of watch dog in case of missing trigger in open window.

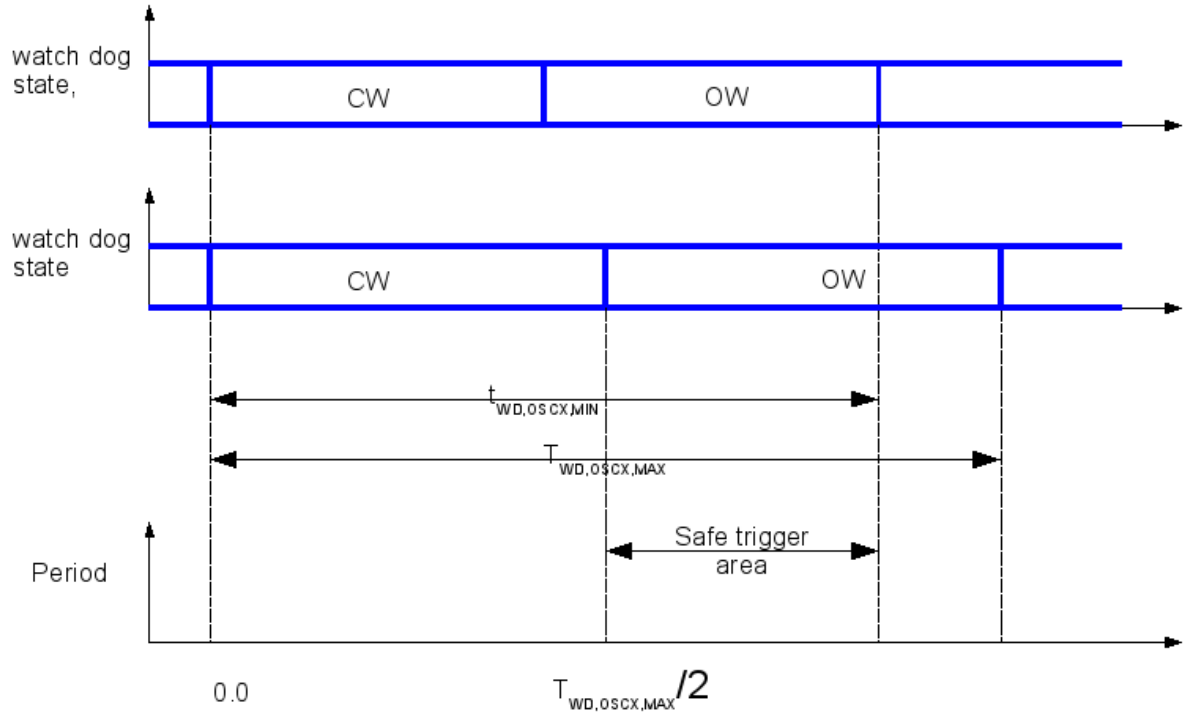


Figure 6.2.6-4: safe trigger area

safe trigger area for a selected watchdog period:

$$STA = T_{WD,OSCX,MIN} - T_{WD,OSCX,MAx}/2$$

6.2.6.1 Watchdog Cycle Time Configuration

The watchdog cycle time can be configured via the external resistor at pin **WDOSC**. The typical watchdog oscillator periods $t_{WD,OSC}$ is defined by the external resistance $R_{WD,OSC}$ by formula:

$$T_{WD,OSCX,MIN} = (R_{WDOSC} - 2k\Omega) * \frac{ms}{k\Omega} * 0.9$$
$$T_{WD,OSCX,MAx} = (R_{WDOSC} + 2k\Omega) * \frac{ms}{k\Omega} * 1.1$$

6.2.6.2 Watchdog Reset

In case a watchdog error appears a reset will be activated on pin **RES_N** for $t_{WD,RES}$.

6.2.6.3 Watchdog Debug Mode

For debugging purposes the watchdog can be stopped running by pulling pin **WDDM** to HIGH. In this case the watchdog timer stops and the actual state remains. After setting pin **WDDM** to low level the watchdog keeps on running.

6.2.7 LIN Transceiver; pin LIN

6.2.7.1 LIN Physical Layer

The LIN BUS physical interface is realized as a LIN 2.1 standard high-voltage single wire interface (ISO 9141) for baud rates from 2.4 kBds to 20 kBds. The LIN BUS Interface can be operated in Master or Slave Mode. The LIN bus has two logical values; the dominant state (BUS voltage near GND) represents logical LOW level and the recessive state (BUS voltage near VS) represents logical HIGH level. In the recessive state the BUS is pulled high by an internal pull-up resistor (typ. 30 kΩ) and a diode in series, so no external pull-up components are required for

slave applications. Master applications require an additional external pull-up resistor and a series diode. The LIN protocol output data stream on the TXD signal is converted into the LIN bus signal through a current limited, wave-shaping low-side driver with control as outlined by the LIN Physical Layer Specification Revision 2.1. The receiver converts the data stream from the bus and outputs it to the pin **RXD**.

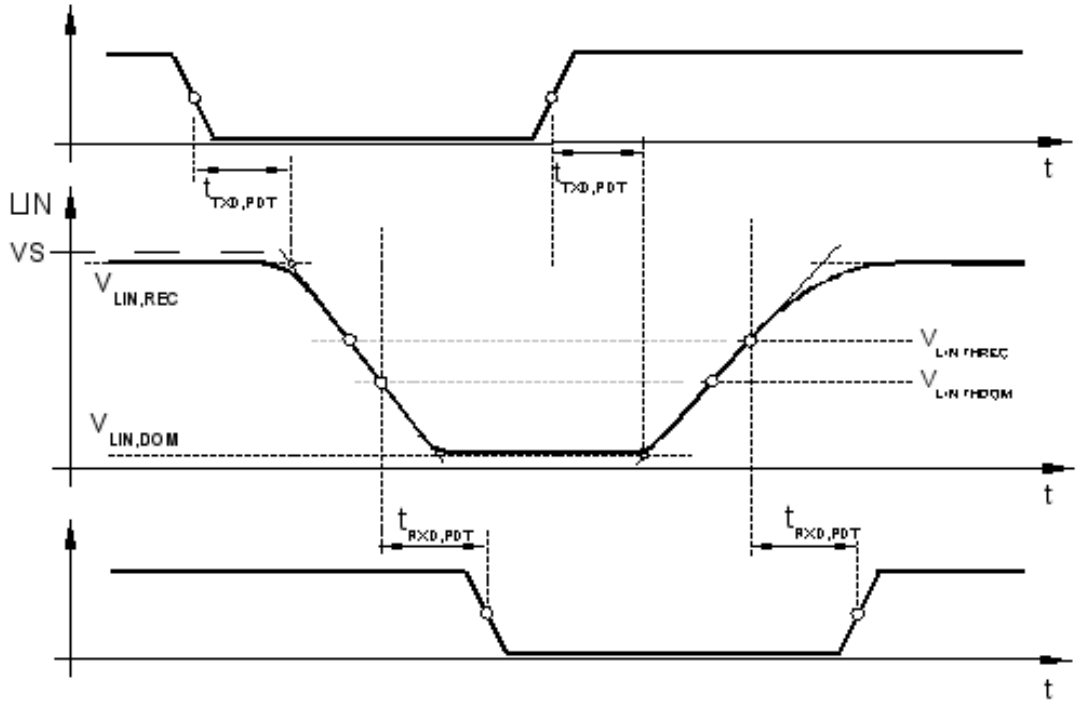


Figure 6.2.7.1-1: LIN transceiver physical layer timing

The LIN transceiver can handle a bus voltage swing from +40 V down to ground and survive -27 V. The device also prevents back feed current through the LIN pin to the supply pin in case of a ground shift / loss or supply voltage disconnection.
In sleep mode the LIN block requires a very low quiescent current by using a special wake up comparator allowing the remote wake-up via the LIN bus. The sleep mode can be activated during recessive or dominant level of LIN bus line.

6.2.7.2 LIN Flash Mode

A Flash mode allows an increasing of the transmit baud rate up to 115 kBaud and the receiver baud rate up to 250 kBaud. The Flash mode can be activated by sending a **TXD** low pulse acknowledge during the Standby mode change caused by **EN** = HIGH.

6.2.7.3 LIN TXD Time Out

In order to prevent the LIN bus from being permanent dominant in case of permanent LOW level at pin **TXD** a TXD time-out timer switches the LIN in recessive mode after time period $t_{TXD,TO}$. The timer is triggered by a negative edge on pin **TXD** and reset by a positive edge on pin **TXD**.

6.2.8 IO Peripherals

6.2.8.1 Enable; pin EN

The input **EN** (enable) controls the state transition together with pin **TXD**. If EN=1 the device enters Active mode after debounce time t_{2AM}.
The enable input is an CMOS level input with pull down resistor $R_{EN,PD}$.

6.2.8.2 Transmit Data Input; pin TXD

The pin **TXD** is the logic level input for transmitting data. The **TXD** time out of time period $t_{TXD,TO}$ for low level input signals prevents the LIN bus to be pulled steadily to GND. The TXD is a CMOS level input.

The pin **TXD** is also an output for wake-up source recognition. It is realized as open drain output with weak pull up resistance to pin **VDD**.

6.2.8.3 Receive Data Output; pin RXD

The pin **RXD** is the logic level receive data output of the LIN Transceiver. It also serves for a host MCU local or remote wake up request.

The pin is an open drain output with pull up resistor connected to pin **VDD**.

6.2.8.4 Reset; pin RES_N

The pin **RES_N** is a system reset output. It resets the host MCU and the watchdog counter in case one of the following reset triggering events occur:

- VDD under voltage reset
- watchdog trigger fail

The reset pin **RES_N** is activated internally by pulling it to low level.
The pin has a pull up resistor connected internally to pin **VDD**.

6.2.8.5 Watchdog Trigger Input; pin WDIN

At pin WDIN the watchdog trigger command has to be launched. The trigger command is a high level pulse of duration $t_{WD,CMD}$. It must not be launched in the watchdog closed window. It must be launched in the watchdog open window.

The pin WDIN is a CMOS level input with pull down current.

6.2.8.6 Watchdog Cycle Time Configuration; pin WDOSC

With logic level pins the watchdog cycle time can be configured by an external resistor.

6.2.8.7 Watchdog Debug Mode; pin WDDM

Setting WDDM to high level stops the watchdog.

The pin **WDDM** is an CMOS level input with pull down current.

6.2.9 VBAT Voltage divider

The pin **DIV_ON** is a low voltage input. It is used to switch on or off the internal voltage divider
PV output directly with no time limitation. It is switched on if DIV_ON is high or it is switched off if DIV_ON is low. In Sleep and Standby Mode the DIV_ON functionality is disabled and PV is off. An internal pull-down resistor is implemented.

The pin **VBAT** is a high voltage input pin to supply the internal voltage divider. In an application with battery voltage monitoring, this pin is connected to Battery via a 47Ω resistor in series and a 10 nF capacitor to GND. The divider ratio is 1:6.

For applications with battery monitoring, this pin **PV** is directly connected to the ADC of a microcontroller. For buffering the ADC input an external capacitor is recommended. This pin guarantees a voltage stable output of a VBAT ratio.

Table 6.2.9-1: table of voltage divider

Mode of Operation	*DIV_ON*	*PV*
ACTIVE, FLASH, POWER ON	0	OFF
ACTIVE, FLASH, POWER ON	1	ON
SLEEP, STANDBY	-	OFF

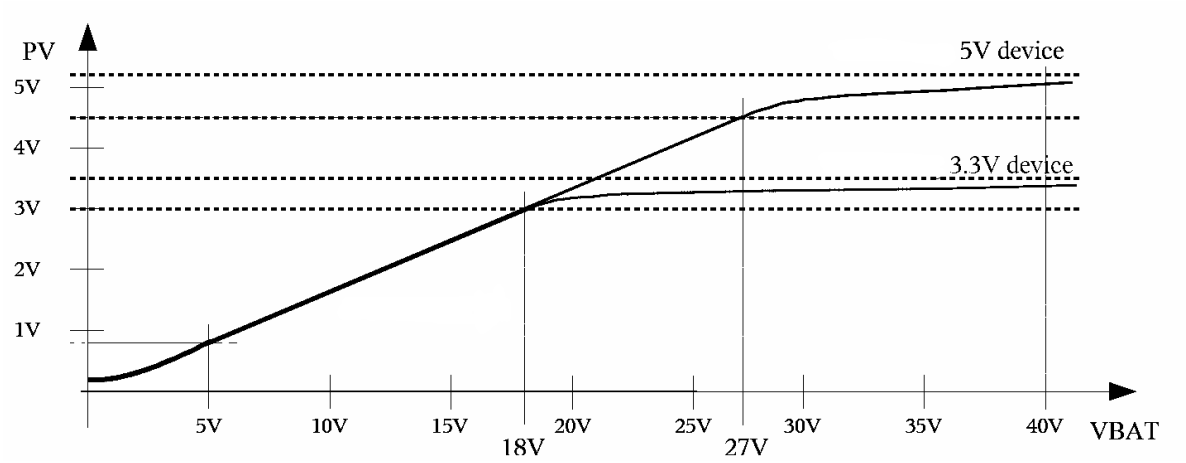


Figure 6.2.9-1: VBAT versus PV

7 Package Reference

The E527.05 is available in a Pb free, RoHs compliant, QFN44L7 plastic package according to JEDEC MO-220 VKKD-3. The package is classified to Moisture Sensitivity Level 3 (MSL 3) according to JEDEC J-STD-020 with a soldering peak temperature of (260+5)°C.

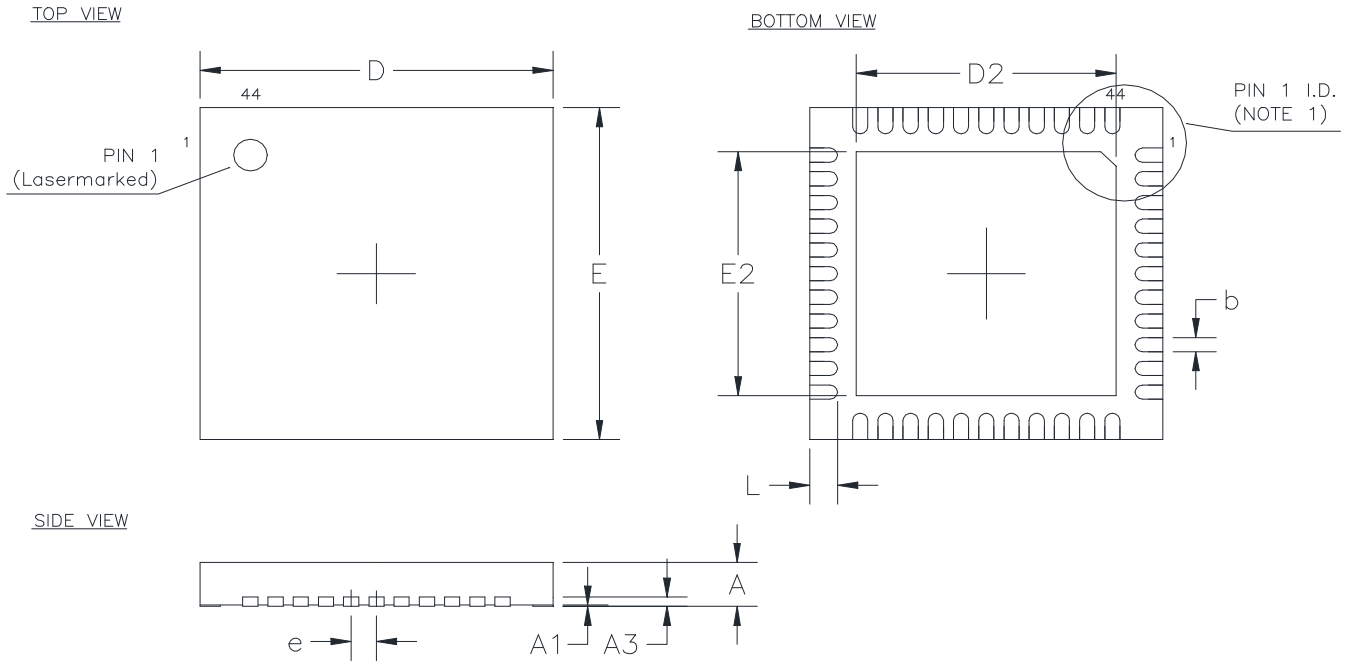


Figure 7-1: Package Outline

Description	Symbol	mm			inch		
		min	typ	max	min	typ	max
Package height	A	0.80	0.90	1.00	0.031	0.035	0.039
Stand off	A1	0.00	0.02	0.05	0.000	0.0008	0.002
Thickness of terminal leads, including lead finish	A3		0.20 REF			0.0079 REF	
Width of terminal leads	b	0.18	0.25	0.30	0.007	0.010	0.012
Package length / width	D / E	--	7.00 BSC	--	--	0.276 BSC	--
Length / width of exposed pad	D2 / E2	5.00	5.15	5.25	0.197	0.203	0.207
Lead pitch	e		0.50 BSC			0.020 BSC	
Length of terminal for soldering to substrate	L	0.45	0.55	0.65	0.018	0.022	0.026
Number of terminal positions	N		44			44	

Note: the mm values are valid, the inch values contains rounding errors
Note: Contact factory for specific location and type of pin 1 identification.

8 Typical Applications

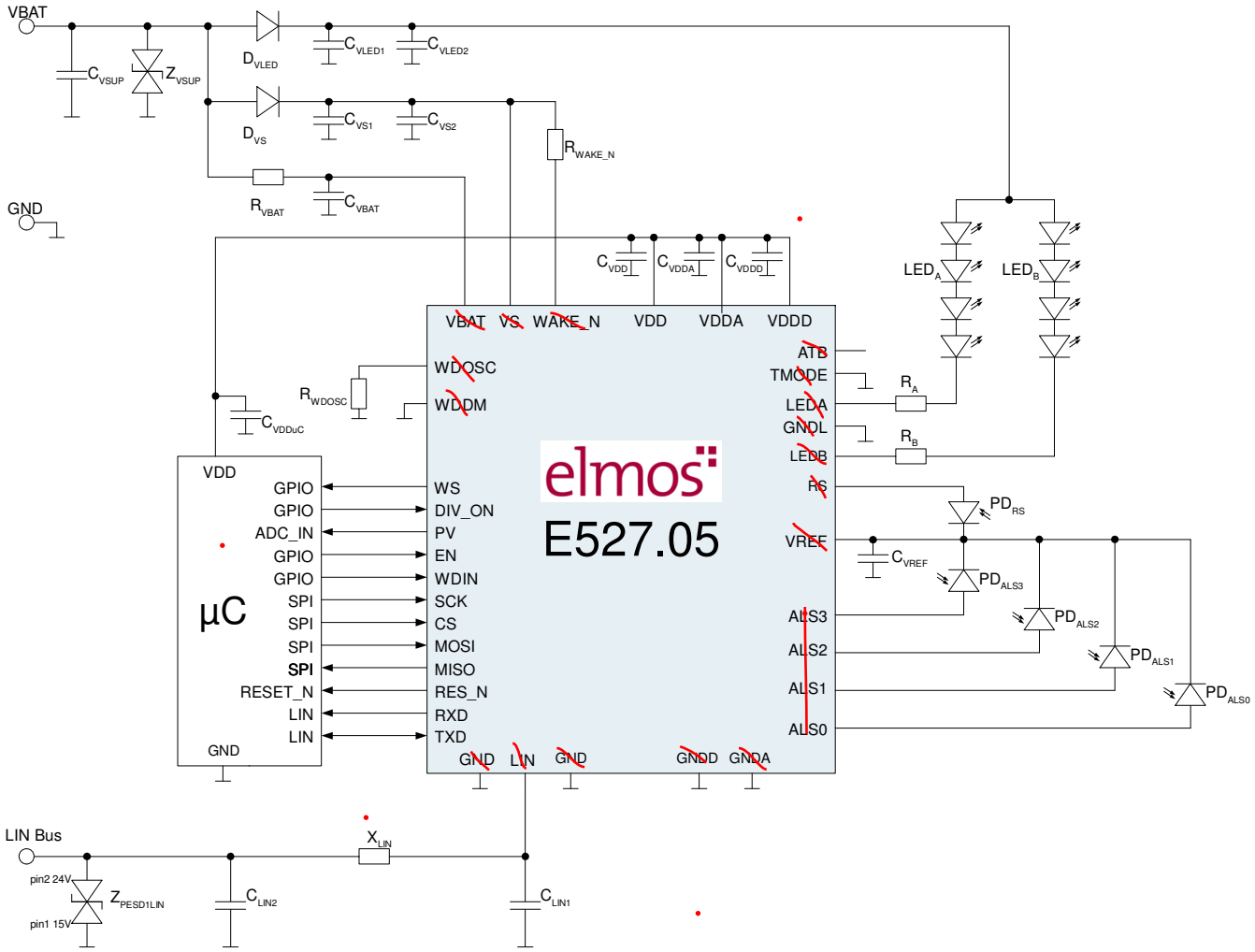


Figure 8-1: Typical Application Example

Table 8-1: External Components

Symbol	Value	Unit	Description
C_{VSUP}	68-100	nF	ESD blocking capacitor, place near module connector.
Z_{VSUP}	43	V	Transient Voltage Suppressor (TVS) diode against over voltage spikes (ESD protection and ISO pulses), e.g. SMAJ36CA or P4S-MA43C(A). Place near module connector.
D_{VLED}, D_{VS}			Reverse polarity protection diode, e.g. BAS521.
R_{VBAT}	47	Ω	ESD protection resistor
C_{VLED1}	100	nF	Blocking capacitor
C_{VLED2}	22	µF	Capacitor to flatten LED current pulses, value could change. Also tank capacitor to supply LEDs during short disconnection of supply wire.
C_{VS1}	100	nF	Blocking capacitor, place near pin VS.

Symbol	*Value*	*Unit*	*Description*
C_{VS2}	min. 22	µF	Blocking capacitor against ISO Pulse 2A. Also tank capacitor to supply circuit during short disconnection of supply wire. Max. autarky (disconnection) time with min. specified VBAT voltage $VBAT_{MIN}$ can be calculated with: $t_{autarky} = C_{VS2} * (VBAT_{MIN} - V_{D\_VS} - V_{S,FUNC\ MIN}) / I_{VS}$. V_{D_VS} is the voltage of diode D_{VS}. I_{VS} is the current into pin VS. $V_{S,FUNC\ MIN}$ is the minimum specified functional range of supply voltage VS.
C_{VBAT}	47	nF	ESD protection capacitor
R_{WAKE_N}	33	kΩ	ESD protection pull up resistor
C_{VDDA}	220	nF	Blocking capacitor, place near pin VDDA
C_{VDDD}	220	nF	Blocking capacitor, place near pin VDDD
C_{VDD}	10	µF	Buffer capacitor
C_{VDDuC}			Blocking capacitor for µC supply, value depends from µC, place near µC supply pin.
R_{WDOSC}			Configures the watchdog cycle time, described in chapter Watchdog.
LED_A, LED_B			SFH4253, SFH4243, VSMF9700, VSMF3710 or similar types, 3 or 4 LEDs per strand recommended.
R_A, R_B			Optional series resistor to reduce power dissipation of 527.05 LED driver, min. voltage at pins LEDA and LEDB is 0.8V.
PD_{RS}			SFH2400 or similar types, capacitance should not be more than 35pF. Place near pin RS and VREF. Net RS is a very sensitive node and should be as short as possible.
PD_{ALSx}			SFH2400, BPW34, TEMD5020, TEMD6010, TEMD6200, TEMD7000 or similar types, capacitance should not be more than 70pF.
C_{VREF}	1	nF	VREF Blocking capacitor
C_{LIN1}	220/180	pF	220pF if C_{LIN2} and $P_{ESD1LIN}$ is not used, 180pF if C_{LIN2} and P_{SD1LIN} is used. By LIN specification the whole capacitance of LIN terminal should be 220pF.
X_{LIN}			0Ω Resistor or optional ferrite to suppress distortion from micro-controller.
C_{LIN2}			Optional capacitor if demanded by OEM.
$Z_{PESD1LIN}$	15/24	V	Optional LIN-bus ESD protection diode PESD1LIN for increased ESD requirements of 8KV. Place near LIN Bus connector.

9 Revision History

Table 9-1: Table of Revisions

Rev.	*Date*	*Description of change*	*Chapter*	*Who*
00	28.05.15	Initial Version	All	BR/ZOE

10 General

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