FS8600_SDS

Fail-safe system basis chip with multiple SMPSs and LDOs

Rev. 3.0 — 4 October 2024 Product short data sheet

1 General description

The FS86 device family, which is software compatible with the FS84/85 family, expands the power capability, the safety integration and the system scalability of domain controller applications to address the multiple MCU requirements present in ADAS, radar and electrification applications.

The FS86 includes multiple switch mode and linear voltage regulators and enhanced safety features with Fail-safe outputs. The latest NXP HV buck architecture features a 15 A capability with e-fuse protection to shut down the system power, to prevent any damage in case of a harmful event. The ability to monitor ten voltages with ±1 % accuracy extends the system safety concept by allowing QM rails from non-NXP components to be monitored.

With its innovative synchronization feature, the FS86 is part of the BYLink system power platform, enabling a new smart approach to designing safe system power management. It provides power, safety and system scalability to ease platform development strategies. Cascaded system SBC/PMICs behave as one with safety and sequencing synchronization.

The FS86 is part of a complete family of devices that offer scalability in power and safety and provide pin-to-pin and software compatibility. It is developed in compliance with the ISO 26262 standard and is qualified according to AEC-Q100 requirements.

2 Features and benefits

Operating Range

- 60 V DC maximum input voltage for 24 V battery network applications
- 36 V DC maximum input voltage for 12 V battery network applications
- Supports operating voltage range down to 4.5 V battery voltage with V_{PRE} = 3.3 V
- Low power OFF mode with low sleep current (10 µA typ.)

Power Supplies

- VPRE: Synchronous high voltage buck controller with external FETs
  - Configurable output voltage from 3.3 V to 5.0 V and current capability up to 15 A DC
  - Selectable switching frequency in force PWM with APS
- BOOST: Low voltage boost converter with integrated low-side FET
  - Configurable output voltage from 5 V to 6 V and current capability up to 1 A DC
- BUCK: Low-voltage integrated synchronous BUCK converter
  - Configurable output voltage from 1.0 V to 3.3 V and current capability up to 2.5 A DC
- LDO1: Low voltage LDO regulator for MCU I/O and system peripheral support with load switch capability
  - Configurable output voltage from 1.5 V to 5.0 V and current capability up to 400 mA DC
- LDO2: Medium voltage LDO regulator for MCU I/O and system peripheral support
  - Configurable output voltage from 1.1 V to 5.0 V and current capability up to 400 mA DC

System support

- 2x input pins for wake-up detection, 3.3 V compatible and battery voltage sensing capability
- Analog multiplexer with full system voltages monitoring
- Enhanced leader/follower power-up sequencing management through XFAILB pin
- 10 ms optional RSTB release delay during power up for certain MCU compliancy
- Device control via 32-bit I^2C interface with 8-bit CRC

Compliancy

- EMC optimization features on switching regulators including spread spectrum, slew rate control and manual frequency tuning
- EMI robustness supporting various automotive EMI Test standards
- Conducted emission: IEC 61967-4
- Conducted immunity: IEC 62132-4
- Radiated emission: FMC1278 rev. 3 from 2018
- Radiated immunity: FMC1278 from 2018 and ISO11452-4

Functional Safety

- Scalable portfolio to fit ASIL B to ASIL D automotive safety systems
- Independent voltage monitoring circuitry
- Up to 10 voltage monitoring inputs for FS86 and external PMIC voltage rails with 1 % target accuracy
- Dedicated interface for MCU monitoring with simple or challenger watchdog monitoring
- MCU hardware failure monitoring with PWM monitoring capability (FCCU)
- External IC failure monitoring (ERRMON)
- Logical and analog built-in self-test (LBIST, ABIST)
- Safety outputs with latent fault detection mechanism (PGOOD, RSTB, FS0B)

Configuration and Enablement

- QFN 48 pins with exposed pad for optimized thermal management

- OTP programming for device customization

3 Applications

- Domain controller (ADAS, electrification, infotainment, etc.)
- Radar (radar, imaging radar)
- Vision (mono camera, stereo camera, night vision, etc.)
- 24 V battery network (60 V maximum): truck, bus, transportation
- 12 V battery network (36 V maximum): automotive

4 Simplified Application Diagram

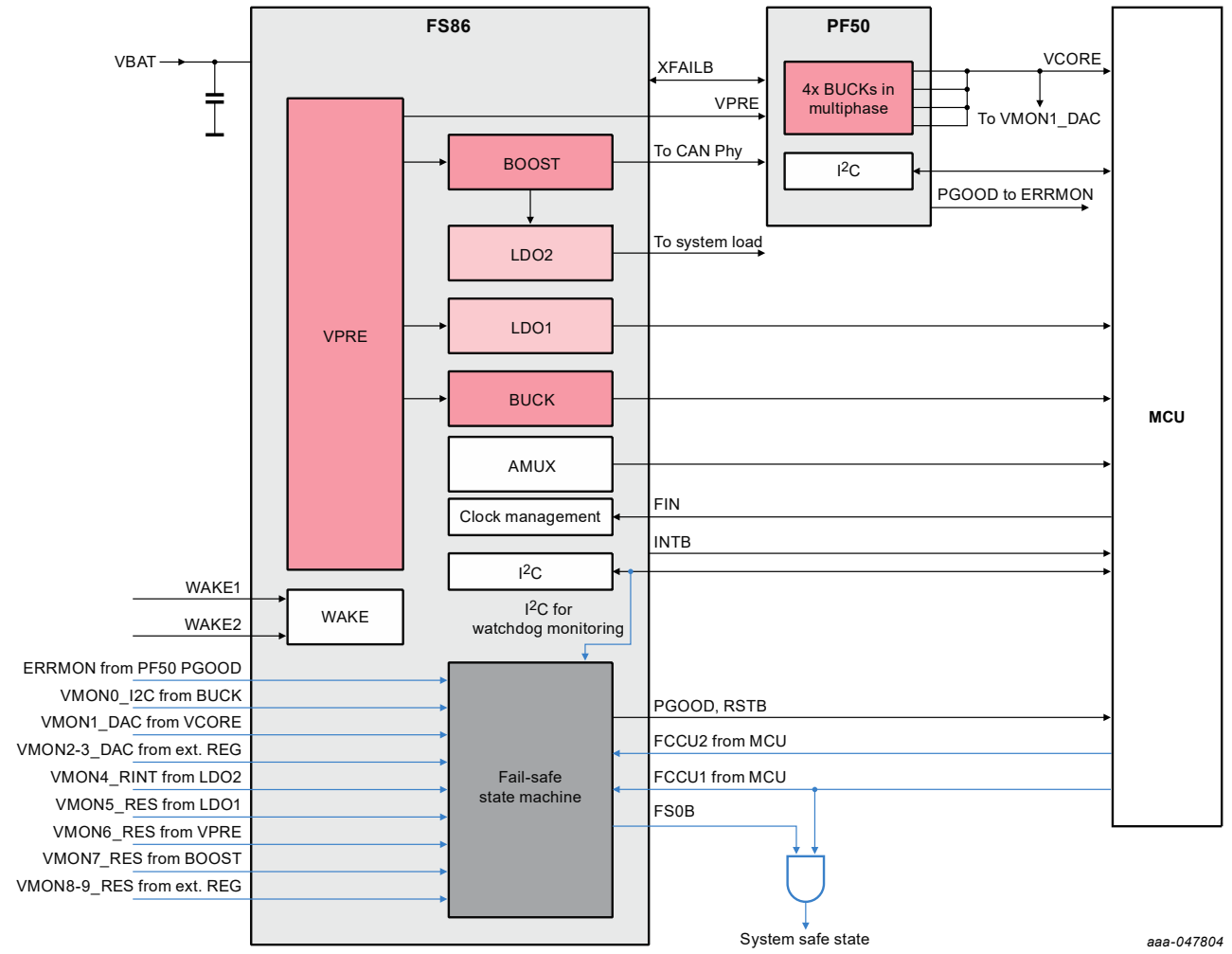

Figure 1. Simplified application diagram

5 Ordering information

5.1 Device family

The FS8600 device family (called FS86 hereafter) provides selectable features based on part numbering and OTP configuration.

Table 1. Device options

FS + Core ID	Application	V_{SUP} max rating	VPRE	BOOST	BUCK	LDOs	VMONs	Watchdog	FCCU	ERRMON	FIN
FS8600	24 V battery network	60 V	Yes	Yes	No	2	4[1]	Yes[2]	Yes	Yes	Yes
FS8601							6[1]				
FS8602							8[1]				
FS8603							10[1]				No[3]
FS8610		60 V	Yes	Yes	Yes	2	4[1]		Yes	Yes	Yes
FS8611							6[1]				
FS8612							8[1]				
FS8613							10[1]				No[3]
FS8620	12 V battery network	36 V	Yes	Yes	No	2	4[1]		Yes	Yes	Yes
FS8621							6[1]				
FS8622							8[1]				
FS8623							10[1]				No[3]
FS8630		36 V	Yes	Yes	Yes	2	4[1]		Yes	Yes	Yes
FS8631							6[1]				
FS8632							8[1]				
FS8633							10[1]				No[3]

[1] Maximum number allowed. Any VMONx can be enabled up to this limit.
[2] ASIL B: watchdog simple. ASIL D: watchdog challenger.
[3] FIN and VMON9 cannot be used at the same time (same pin)

5.2 Part numbering

M	FS	8600	B	M	B	A0	ES
P: prototype M: standard S: custom	HV PMIC	FS86 Core ID[1]	Silicon revision A: A0 B: A1	Ambient temperature (T_A) M: –40 °C to 125 °C	ASIL B: ASIL B D: ASIL D	OTP code A0: OTP A0 xx: OTP xx	Package type ES: dimple wettable flank

[1] See Table 1

Table 2. Ordering information

Part Number[1]	Application	Fit for ASIL	Package		
			Name	Description	Version
MFS8600BMBA0ES	24 V battery network	B	HPQFN48eP	HPQFN48, plastic, thermally enhanced very thin quad flat package, no lead, wettable flanks	SOT619-26
MFS8601BMBA0ES					
MFS8602BMBA0ES					
MFS8603BMBA0ES					

Table 2. Ordering information...*continued*

Part Number[1]	Application	Fit for ASIL	Package		
			Name	Description	Version
MFS8610BMBA0ES	12 V battery network				
MFS8611BMBA0ES					
MFS8612BMBA0ES					
MFS8613BMBA0ES					
MFS8600BMDA0ES		D			
MFS8601BMDA0ES					
MFS8602BMDA0ES					
MFS8603BMDA0ES					
MFS8610BMDA0ES					
MFS8611BMDA0ES					
MFS8612BMDA0ES					
MFS8613BMDA0ES					
MFS8620BMBA0ES		B			
MFS8621BMBA0ES					
MFS8622BMBA0ES					
MFS8623BMBA0ES					
MFS8630BMBA0ES					
MFS8631BMBA0ES					
MFS8632BMBA0ES					
MFS8633BMBA0ES					
MFS8620BMDA0ES		D			
MFS8621BMDA0ES					
MFS8622BMDA0ES					
MFS8623BMDA0ES					
MFS8630BMDA0ES					
MFS8631BMDA0ES					
MFS8632BMDA0ES					
MFS8633BMDA0ES					
MFS8620BMDA8ES					
PFS8613AMDA0ES[2]	12 V or 24 V battery network	B or D			
PFS8613BMDA0ES[3]					

[1] To order parts in tape and reel, add the R2 suffix to the part number.
[2] Superset part number that can cover all features for prototype ordering (A0 silicon pass/obsolete).
[3] Superset part number that can cover all features for prototype ordering (A1 silicon pass).

Part numbers ending with the A0 OTP code are non-programmed OTP configuration. Pre-programmed OTP configurations are managed through part number extension. For a custom OTP configuration, contact your local NXP sales representative.

OTP emulation and programming performed by the customer is allowed during engineering development using NXP's latest graphical user interface and socketed evaluation board.

Customer is not allowed to perform OTP programming for production purposes. Only NXP or a recommended third party are allowed to program the device for production purposes.

6 Internal block diagram

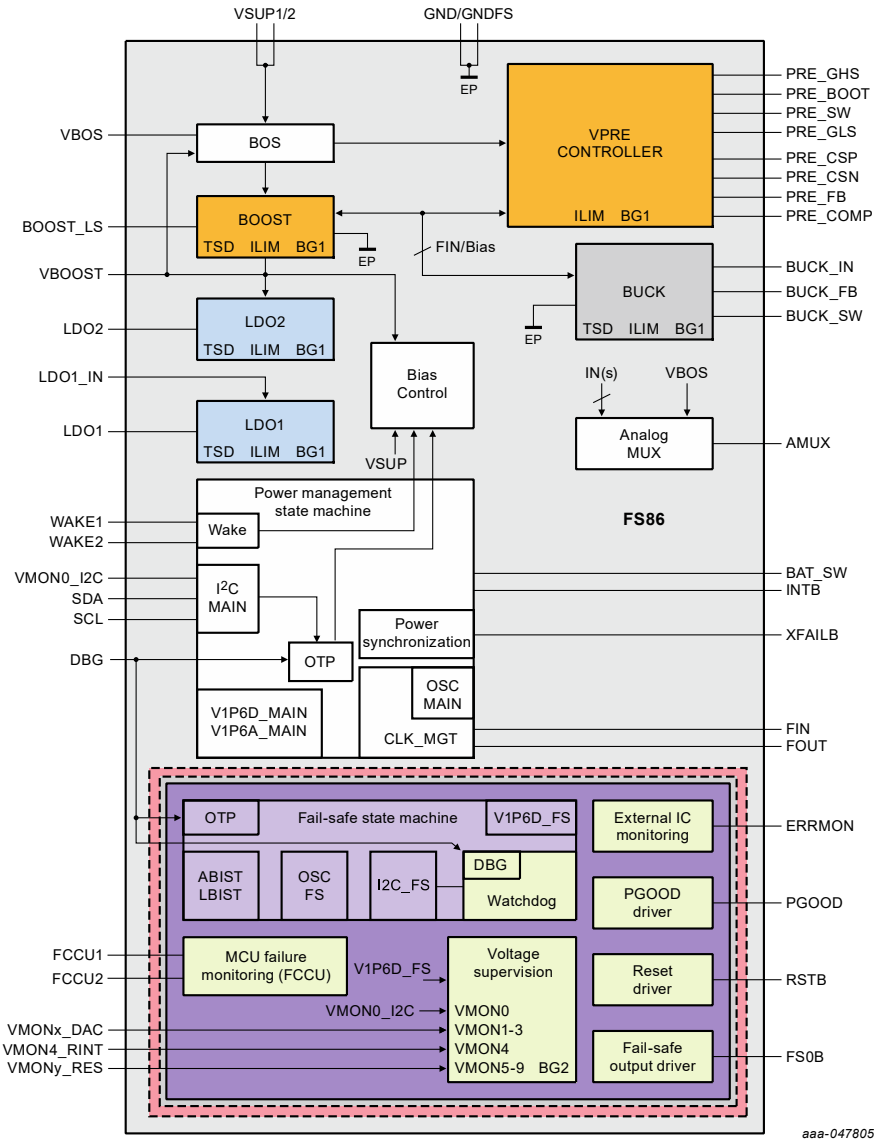

Figure 2. Block diagram

7 Pinout information

7.1 Pinout

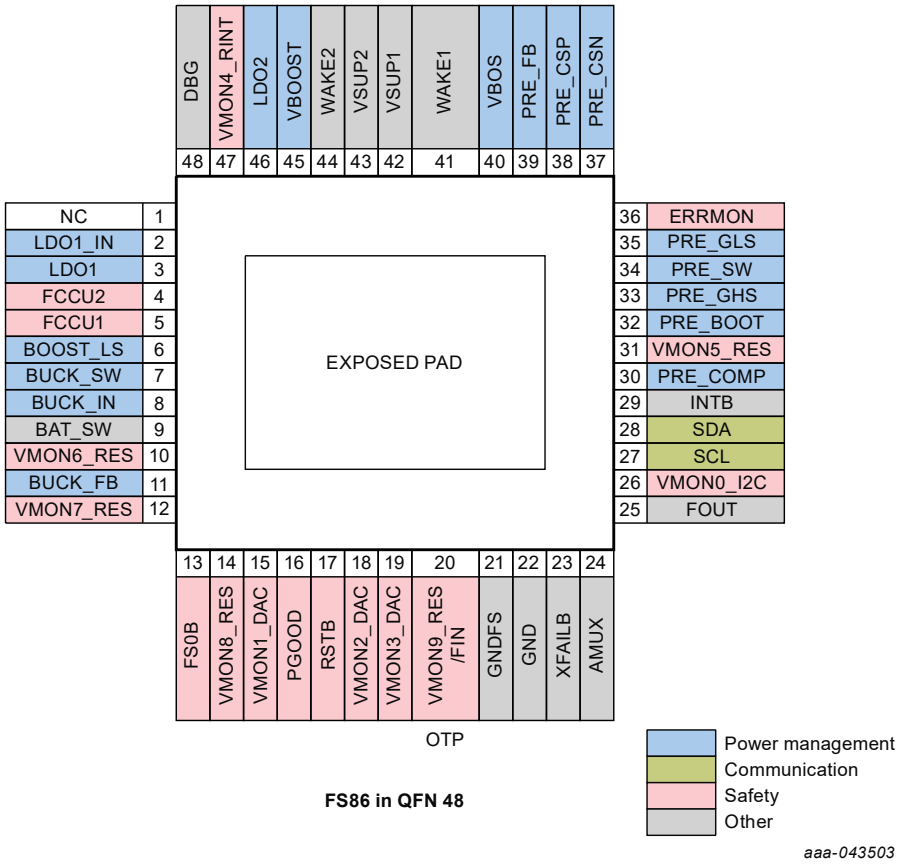

Figure 3. Pin configuration

7.2 Pin description

Table 3. Pin description

Pin	Name	Type	Description
1	N/C	N/C	Not connected pin
2	LDO1_IN	Analog input	Linear regulator #1 input voltage
3	LDO1	Analog output	Linear regulator #1 output voltage
4	FCCU2	Digital input	MCU Error Monitoring input 2
5	FCCU1	Digital input	MCU Error Monitoring input 1
6	BOOST_LS	Analog input	BOOST Low Side Drain of internal MOSFET
7	BUCK_SW	Analog output	Low voltage buck switching node
8	BUCK_IN	Analog input	Low voltage buck input voltage
9	BAT_SW	Digital output	Battery switch control output. Active low. Open drain structure.
10	VMON6_RES	Analog input	External resistor bridge voltage monitoring input #6

Table 3. Pin description...*continued*

Pin	Name	Type	Description
11	BUCK_FB	Analog input	Low voltage buck voltage feedback.
12	VMON7_RES	Analog input	External resistor bridge voltage monitoring input #7
13	FS0B	Digital output	Fail-safe output 0. Active low. Open drain structure.
14	VMON8_RES	Analog input	External resistor bridge voltage monitoring input #8
15	VMON1_DAC	Analog input	DAC voltage monitoring input #1
16	PGOOD	Digital output	Power good output
17	RSTB	Digital input/output	Reset output. Active low. The main function is to reset the MCU. Reset input voltage is monitored in order to detected external reset and fault condition.
18	VMON2_DAC	Analog input	DAC voltage monitoring input #2
19	VMON3_DAC	Analog input	DAC voltage monitoring input #3
20	VMON9_RES	Analog input	External resistor bridge voltage monitoring input #9. Exclusive with FIN (OTP)
20	FIN	Digital input	Frequency synchronization input. Exclusive with VMON9_RES (OTP)
21	GNDFS	Ground	Fail-safe ground
22	GND	Ground	Main ground
23	XFAILB	Digital input/output	Power synchronization input/output with NXP low voltage PMIC
24	AMUX	Analog output	Multiplexed output to be connected to an MCU ADC with selection of the analog parameter thru I^2C.
25	FOUT	Digital output	Frequency synchronization output or digital output (OTP)
26	VMON0_I2C	Analog input	Input voltage for FIN, AMUX, I^2C, INTB, FCCU, ERRMON. Internal resistor bridge voltage monitoring input #0
27	SCL	Digital input	I^2C Bus. Clock input
28	SDA	Digital input/output	I^2C Bus. Bidirectional data line
29	INTB	Digital output	Interrupt output
30	PRE_COMP	Analog input	VPRE compensation network and negative current sense input
31	VMON5_RES	Analog input	External resistor bridge voltage monitoring input #5
32	PRE_BOOT	Analog input/output	VPRE bootstrap capacitor
33	PRE_GHS	Analog output	VPRE high-side gate driver for external MOSFET
34	PRE_SW	Analog output	VPRE switching node
35	PRE_GLS	Analog output	VPRE low-side gate driver for external MOSFET
36	ERRMON	Digital input	External IC error monitoring input
37	PRE_CSN	Analog input	VPRE negative current sense input
38	PRE_CSP	Analog input	VPRE positive current sense input
39	PRE_FB	Analog input	VPRE voltage feedback.
40	VBOS	Analog output	Best of supply output voltage
41	WAKE1	Digital/Analog input	Wakeup input 1 (thru ext. serial resistor)

Table 3. Pin description...*continued*

Pin	Name	Type	Description
42	VSUP1	Power Analog Input	Power supply of the device #1. An external reverse battery protection diode in series is mandatory
43	VSUP2	Power Analog Input	Power supply of the device #2. An external reverse battery protection diode in series is mandatory
44	WAKE2	Digital/Analog input	Wake up input 2 (thru ext. serial resistor)
45	VBOOST	Analog output	Boost output voltage
46	LDO2	Analog output	Linear regulator #2 output voltage
47	VMON4_RINT	Analog input	Internal resistor bridge voltage monitoring input #4
48	DBG	Analog input	DEBUG Mode entry and OTP input supply
EP	EP	Ground	Exposed pad must be connected to GND

8 Maximum ratings

Table 4. Maximum ratings

All voltages are with respect to ground, unless otherwise noted. Exceeding these ratings may cause a malfunction or permanent damage to the device.

Symbol	Conditions	Parameter	Min	Max	Unit
Voltage ratings of 24 V network application part numbers (see Table 2)					
VSUP1/2	DC voltage	VSUP1,2 pins	−0.3	60	V
WAKE1/2	DC voltage	WAKE1,2 pins (external series resistor mandatory)	−1.0	60	V
FS0B	DC voltage	FS0B pin	−0.3	60	V
BAT_SW	DC voltage	BAT_SW pin	−0.3	60	V
PRE_SW	DC voltage	PRE_SW pin	−2.0	60	V
	Transient voltage < 20 ns		−3.0	60	
PRE_GHS, PRE_BOOT	DC voltage	PRE_GHS, PRE_BOOT pins	−0.3	65.5	V
Voltage ratings of 12 V network application part numbers (see Table 2)					
VSUP1/2	DC voltage	VSUP1,2 pins	−0.3	36	V
WAKE1/2	DC voltage	WAKE1,2 pins (external series resistor mandatory)	−1.0	36	V
FS0B	DC voltage	FS0B pin	−0.3	36	V
BAT_SW	DC voltage	BAT_SW pin	−0.3	36	V
PRE_SW	DC voltage	PRE_SW pin	−2.0	36	V
	Transient voltage < 20 ns		−3.0	36	
PRE_GHS, PRE_BOOT	DC voltage	PRE_GHS, PRE_BOOT pins	−0.3	41.5	V
Voltage ratings of general pins					
BOOST_LS	DC voltage	BOOST_LS pin	−0.3	8.5	V
VBOOST	DC voltage	VBOOST pin	−0.3	6.5	V
BUCK_IN	DC voltage	BUCK_IN pin	−1.0	5.5	V
	Transient voltage < 3 µs		−1.0	6.5	
BUCK_SW	Transient voltage < 20 ns	BUCK_SW pin	−0.3	6.5	V
VMONx	DC voltage	VMONx_DAC 1-3, VMONy_RES 5-9	−0.3	36	V
DBG	DC voltage	DBG pin	−0.3	10	V
All other pins	DC voltage	at all other pins	−0.3	5.5	V

9 Electrostatic discharge

9.1 Human body model (JESD22/A114)

The device is protected up to ±2 kV, according to the human body model standard with 100 pF and 1.5 kΩ. This protection is ensured at all pins.

9.2 Charged device model

The device is protected up to ±750 V on corner pins and up to ±500 V on all other pins, according to the AEC Q100 - 011 charged device model standard.

9.3 Discharged contact test

The device is protected up to ±8 kV, according to the following discharged contact tests.

- Discharged contact test (IEC61000-4-2) at 150 pF and 330 Ω
- Discharged contact test (ISO10605.2008) at 150 pF and 2 kΩ
- Discharged contact test (ISO10605.2008) at 330 pF and 2 kΩ

This protection is ensured at the VSUP1, VSUP2, WAKE1, WAKE2, and FS0B pins.

10 Thermal ratings

Table 5. Thermal ratings

Symbol	Description (Rating)	Min	Max	Unit
Thermal ratings				
T_A	Ambient temperature (Grade 1)	−40	125	°C
T_J	Junction temperature (Grade 1)	−40	150	°C
T_{STG}	Storage temperature	−55	150	°C
Thermal resistance (per JEDEC JESD51-2 and JESD51-8)				
$R_{\theta JA}$	Thermal resistance junction to ambient (2s2p)	—	31	°C/W
$R_{\theta JA}$	Thermal resistance junction to ambient (2s6p)	—	23	°C/W
$R_{\theta JB}$	Thermal resistance junction to board (2s2p)	—	15	°C/W
$R_{\theta JB}$	Thermal resistance junction to board (2s6p)	—	10	°C/W
$R_{\theta JC\_BOT}$	Thermal resistance junction to case bottom (between the die and the solder pad on the bottom of the package)	—	1	°C/W
$R_{\theta JP\_TOP}$	Thermal resistance junction to package top (between package top and the junction temperature)	—	3	°C/W

11 Revision history

Document ID	Release date	Description
FS8600_SDS v3.0	4 October 2024	• This revision synchronizes the short data sheet with the v3.0 full data sheet • Product data sheet • Global: corrected capitalization of *Fail-safe* • Global: corrected formatting of I^2C, applying superscript when it is not part of another name • Updated Table 1 • Updated Table 2 • Updated Section 5.2: added statement about OTP emulation and programming • Updated Figure 2 • Updated legal information
FS8600_SDS v2.0	7 December 2022	• Product data sheet • CIN 202212001I • Updated Section 1 • Updated Section 2 • Updated Table 1 footnotes • Updated Figure 2 • In the VMONx row of Table 4, changed VMON_RES to VMONy_RES
FS8600_SDS v1.1	23 November 2021	• Initial release of product data sheet

Legal information

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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